

Compal Confidential

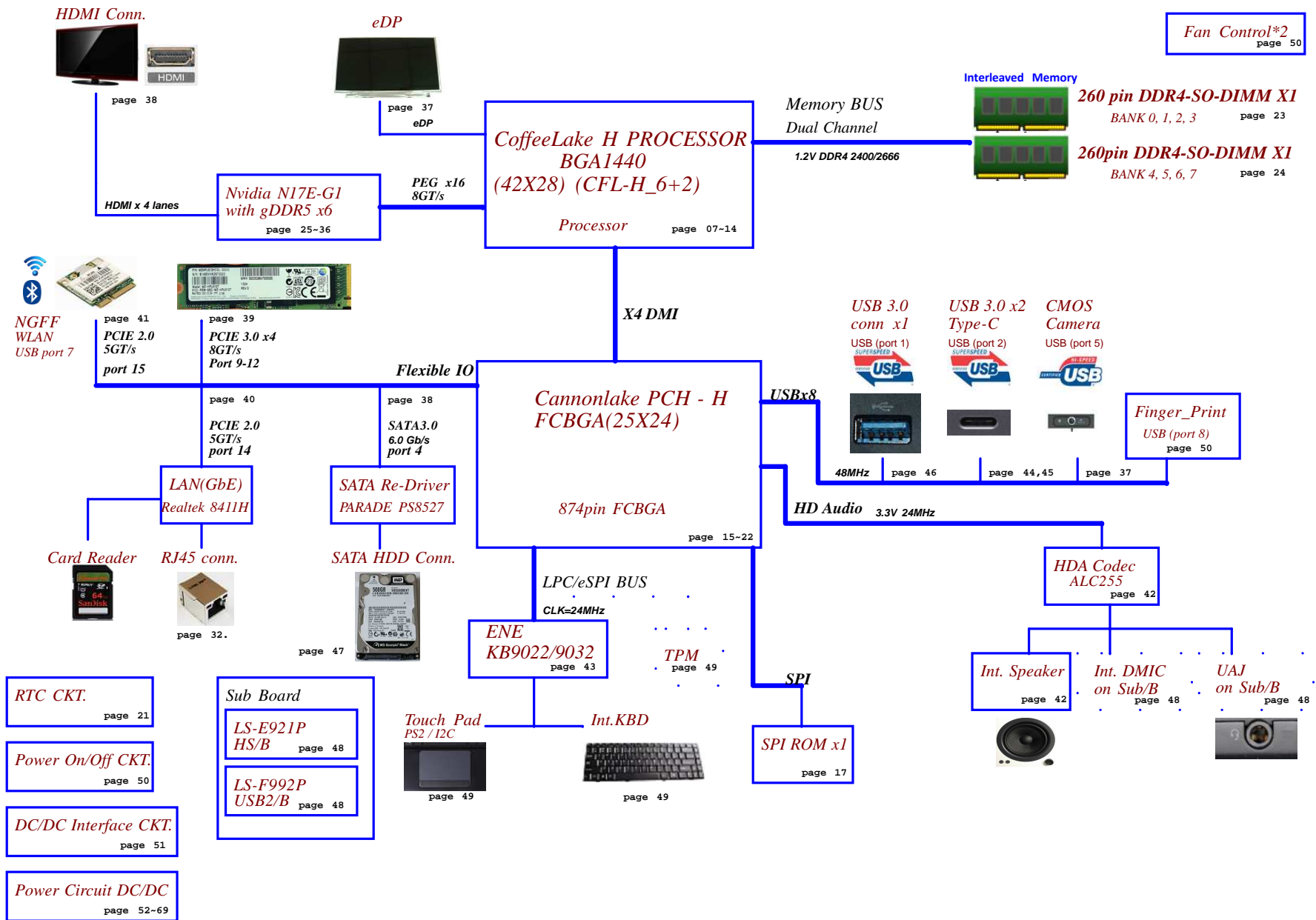
DH53F MB Schematic Document

LA-F991P

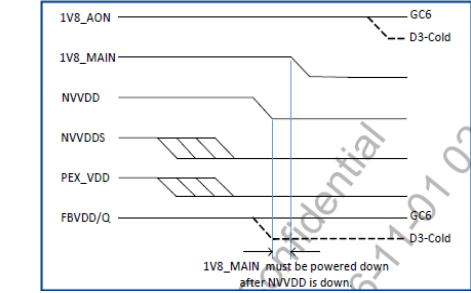
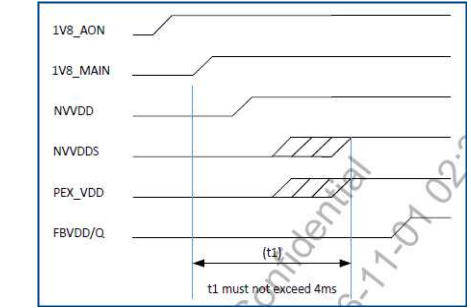
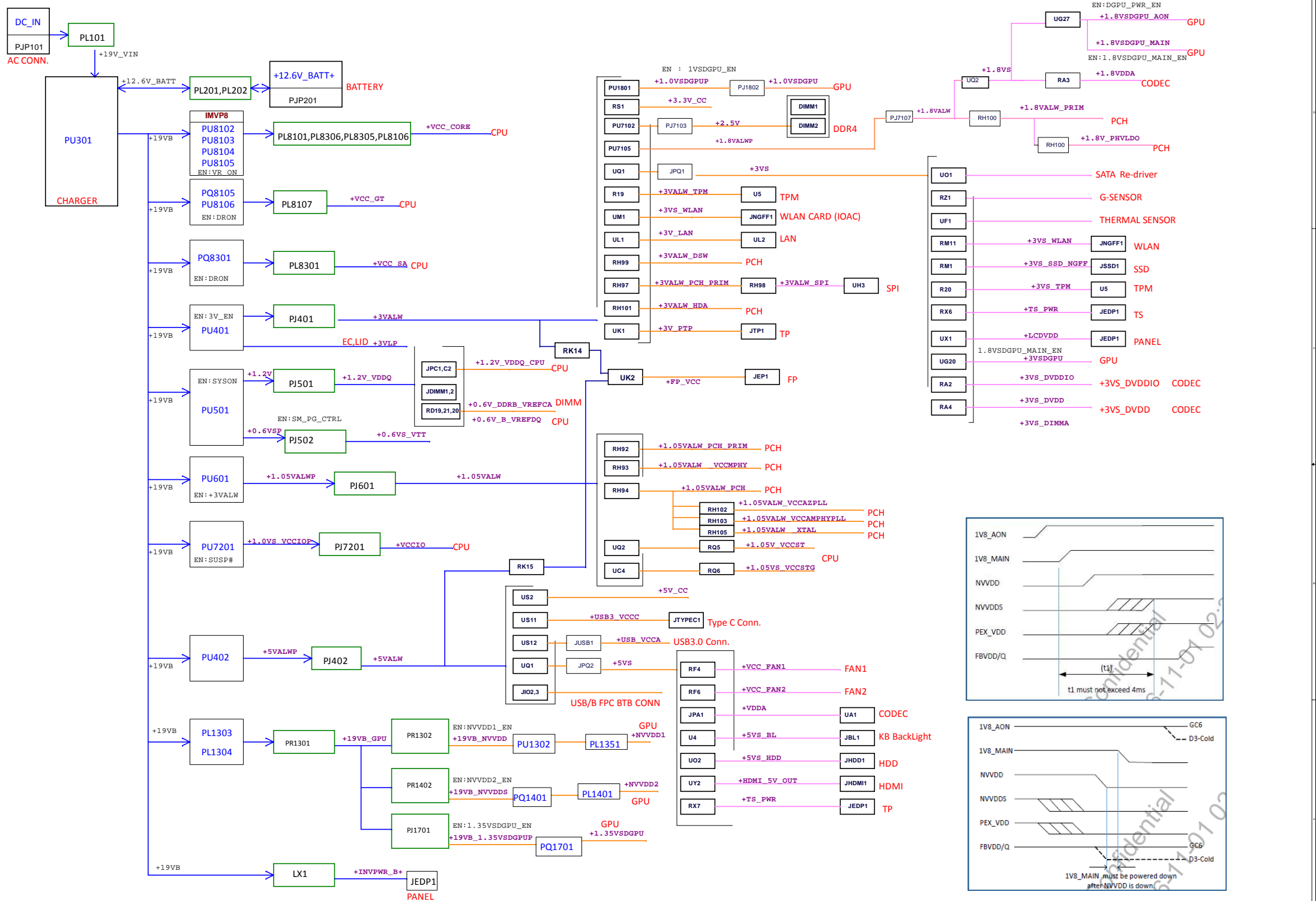
Rev : 1.C

2018.02.13

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|---|------------|--------------------|------------|----------------------------------|---------------------------------------|
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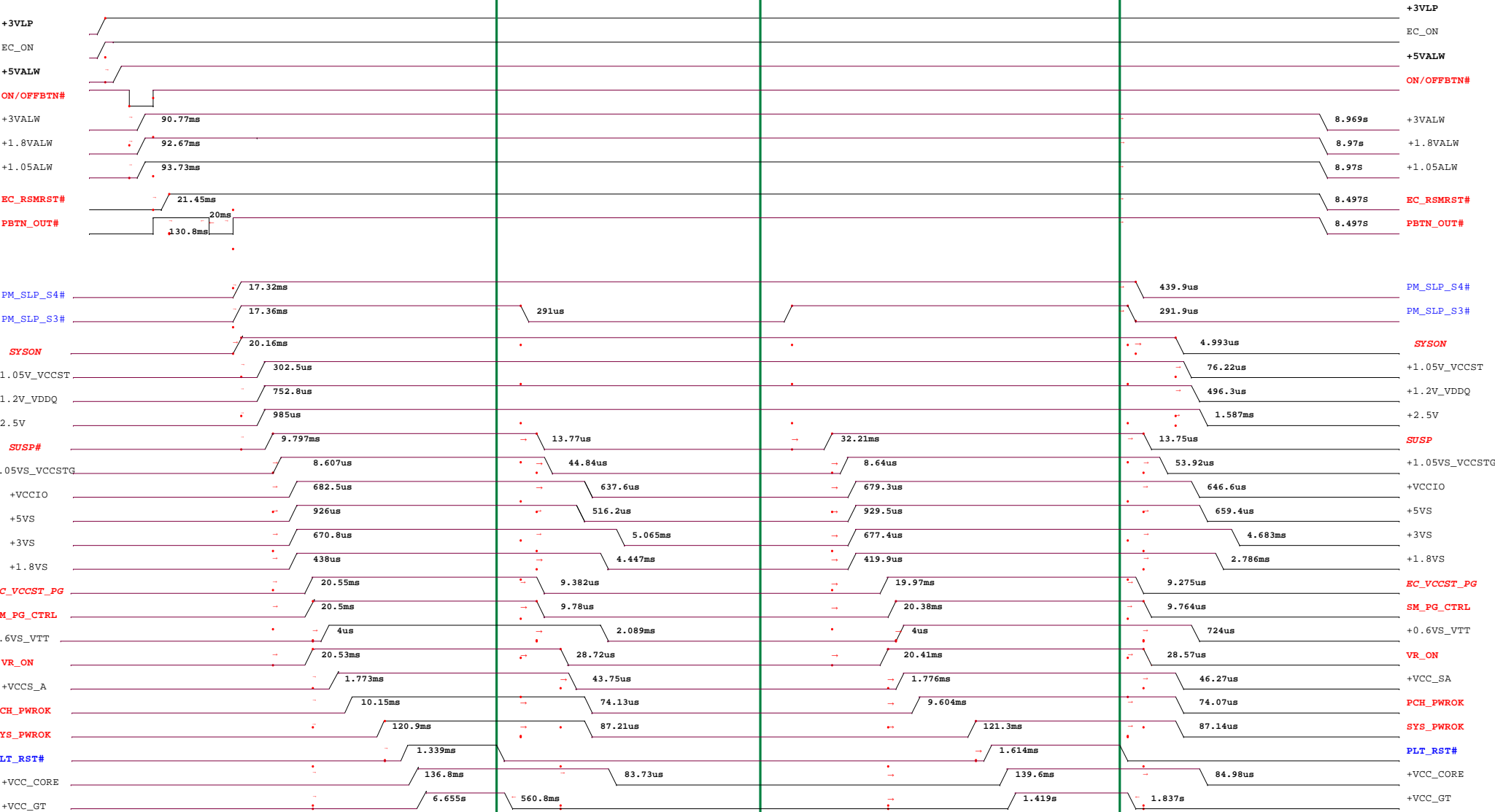
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DH53F_EVT Power Sequence

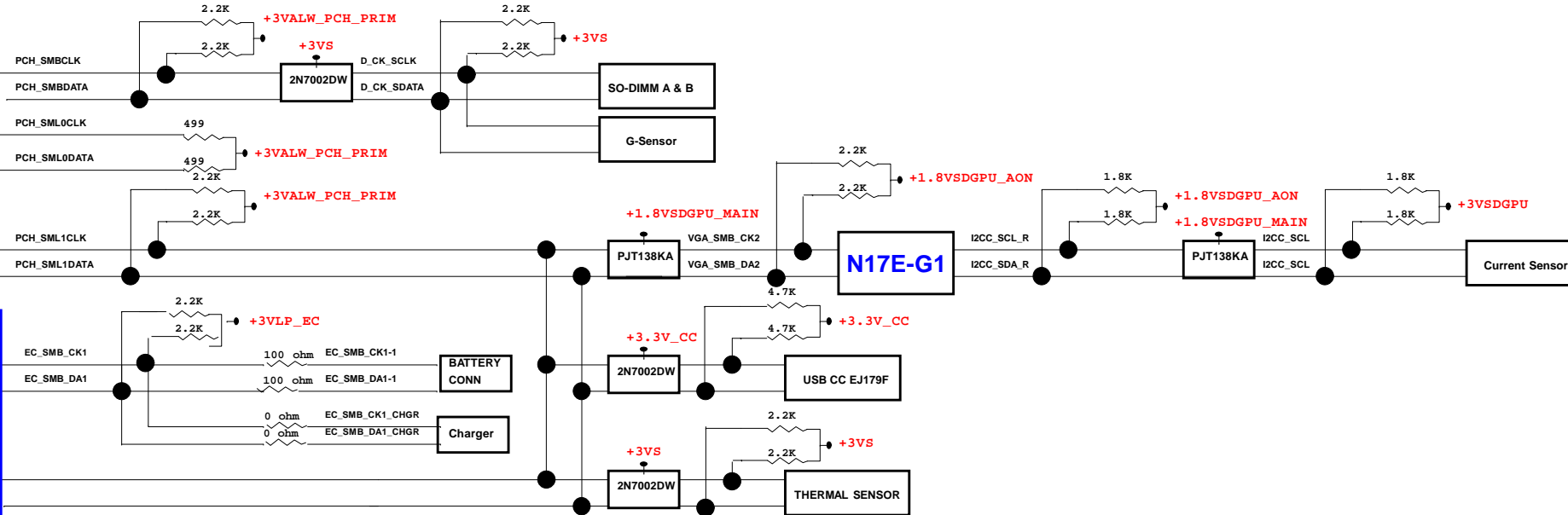
BIOS : 0.05
AC mode

Plug in



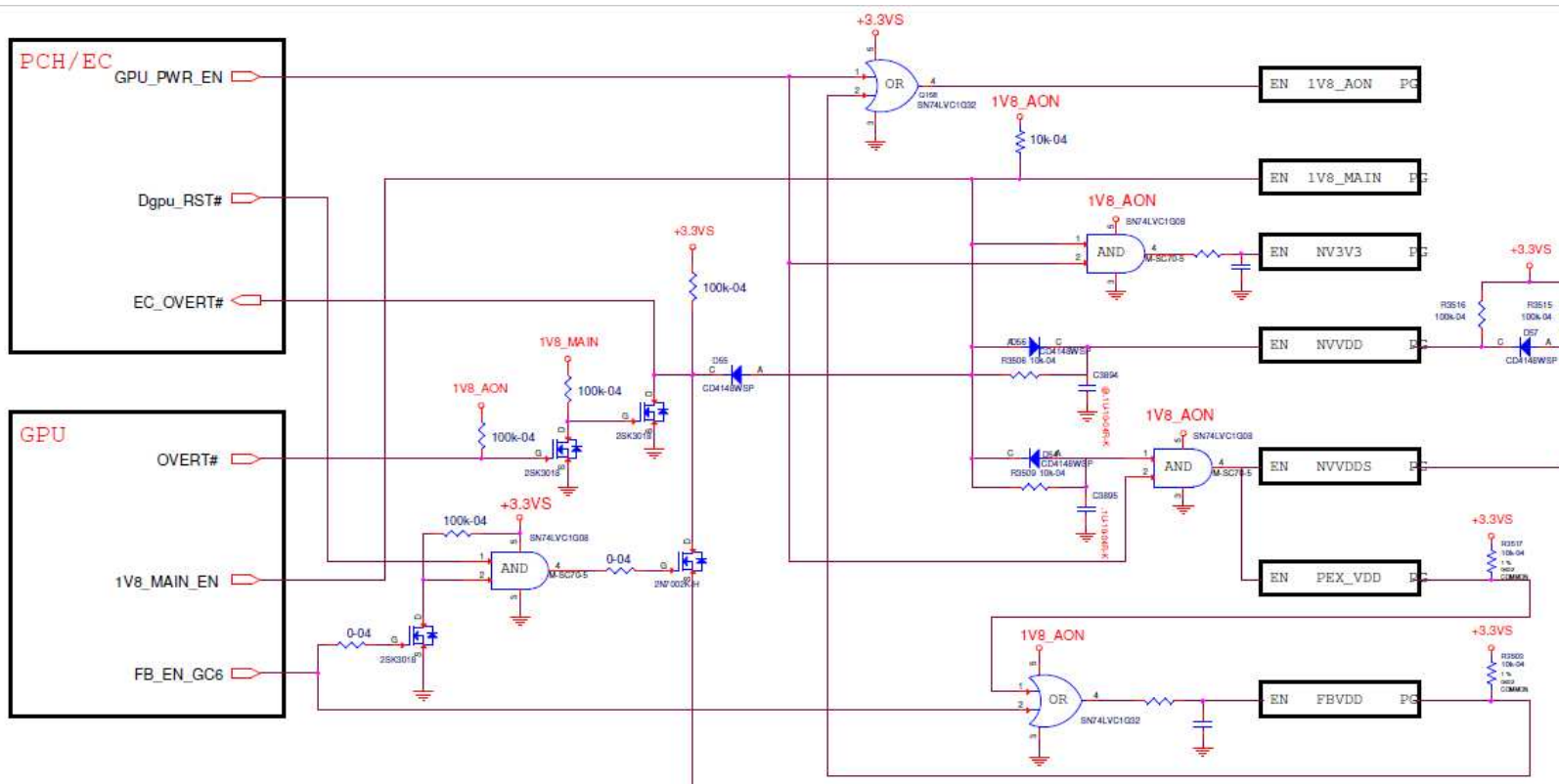
CannonLake-H
PCH

KB9022



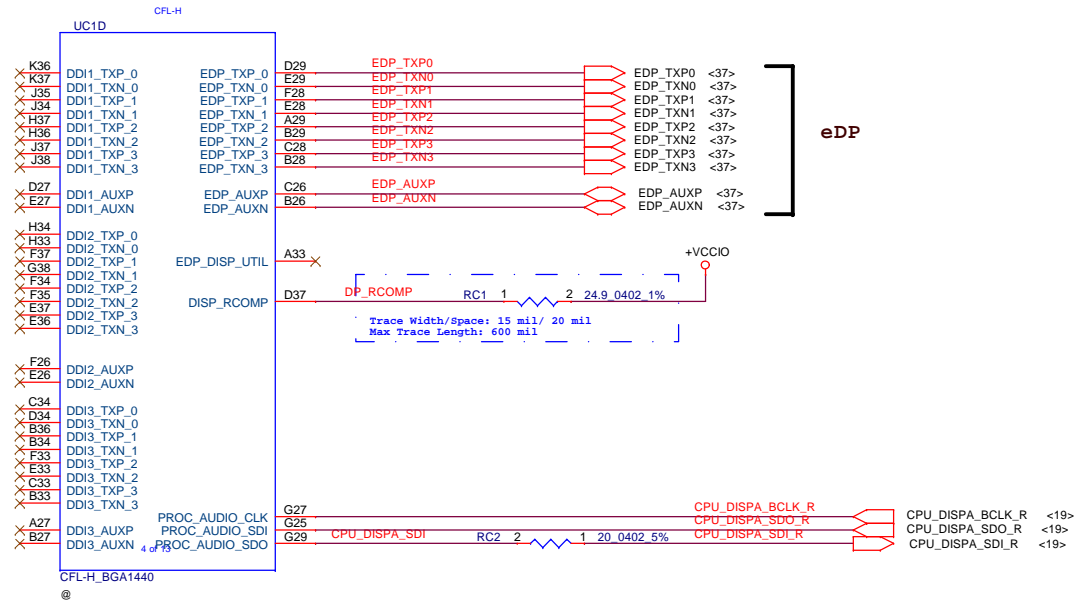
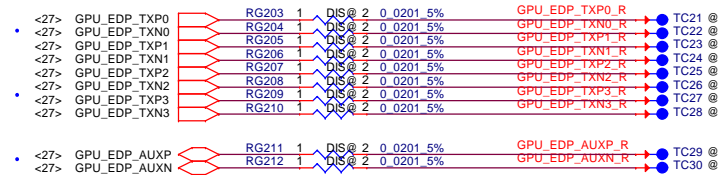
PCH/EC

GPU



| | | | | |
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CO-LAY FOR VGA OUTPUT



ZZZ

PCB@ DAZ29000103

PCB DH53F LA-F991P LS-F992P/E921P

Coffee Lake-H CPU SKU

UC1

CFL-H_BGA1440

S IC CL8068403373522 SR3Z0 U0 2.3G ABO!

SA0000BPJ40

I5@

UC1

CFL-H_BGA1440

S IC CL8068403359524 SR3YY U0 2.2G ABO!

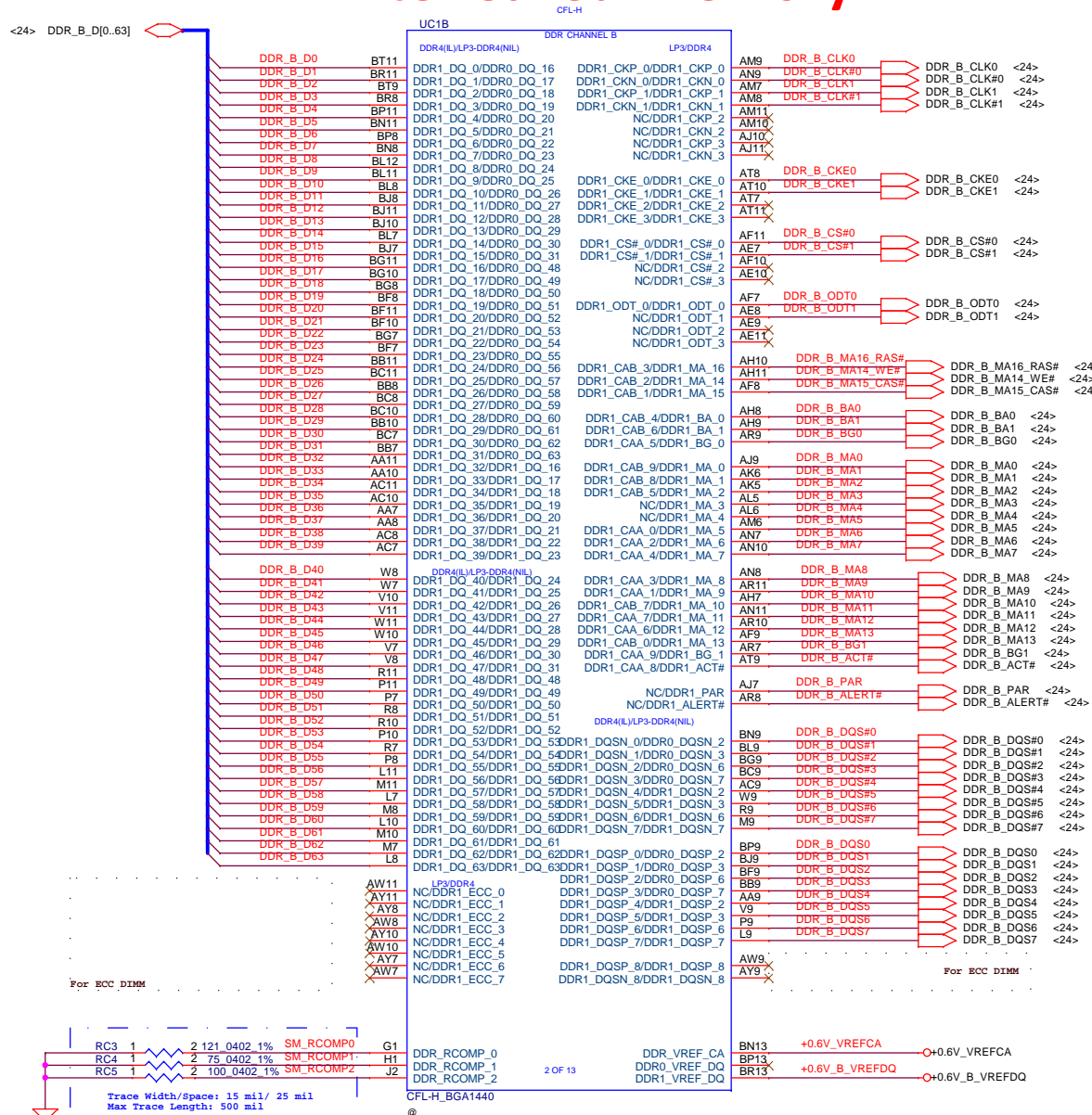
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I7@

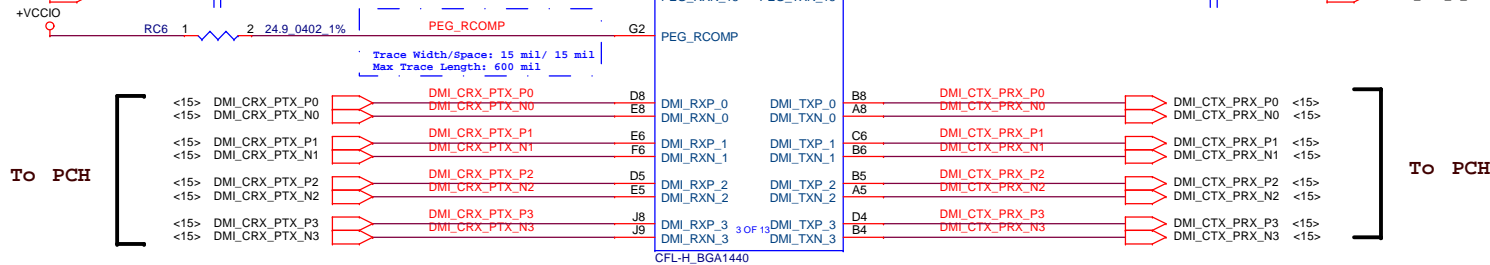
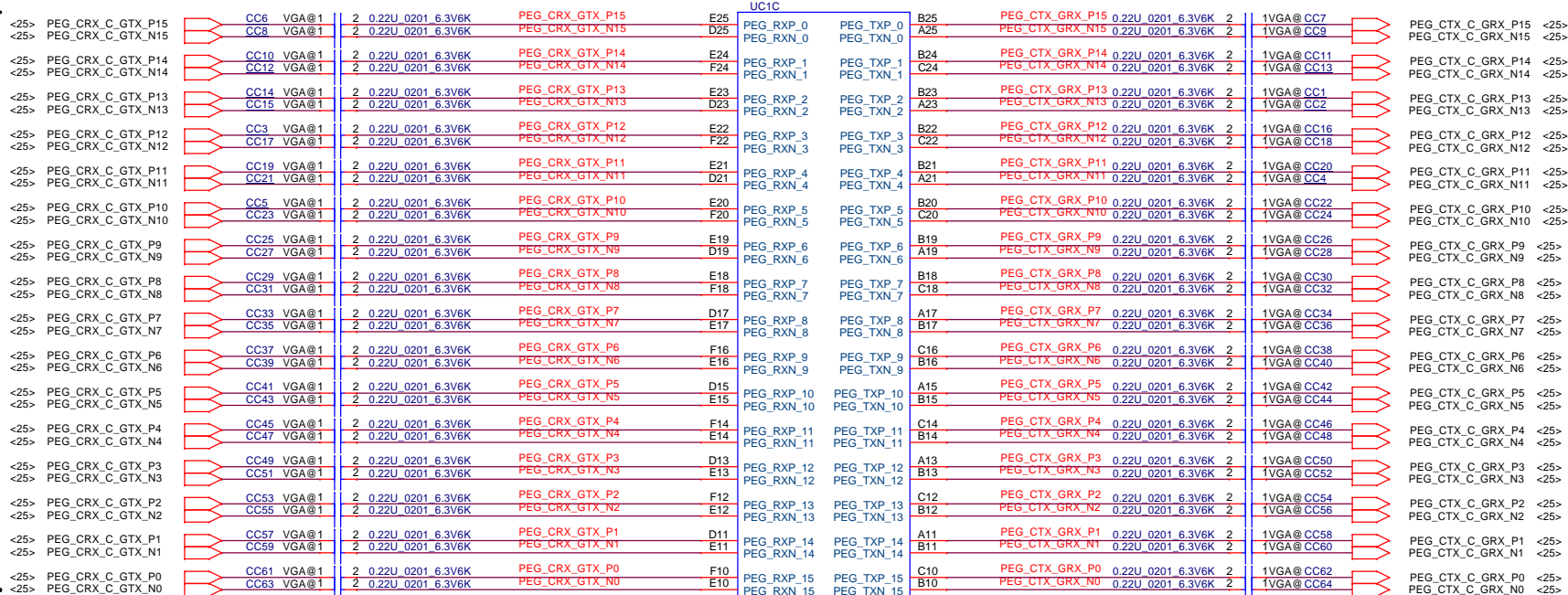
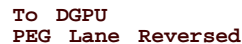
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CHANNEL-B

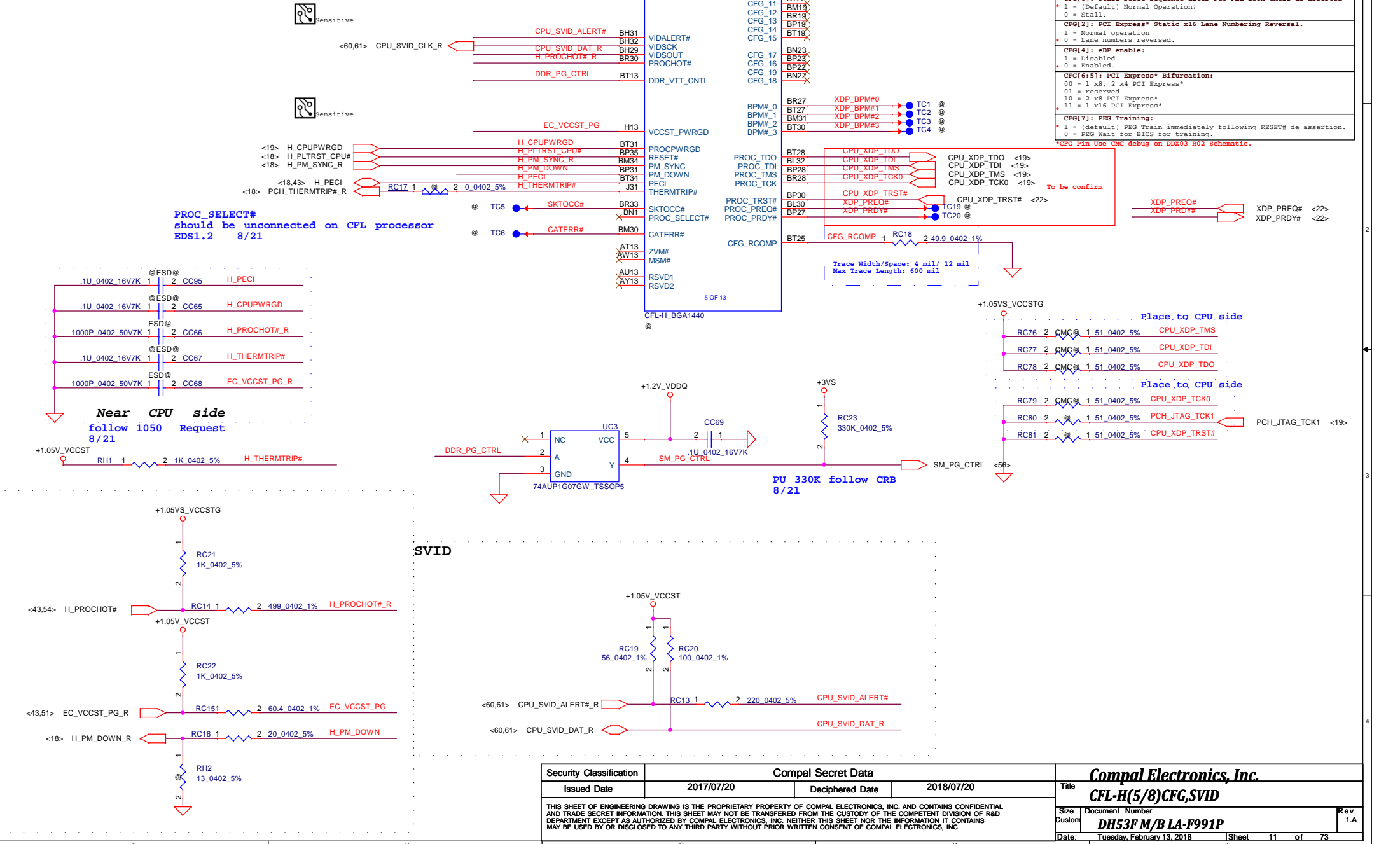
Interleaved Memory



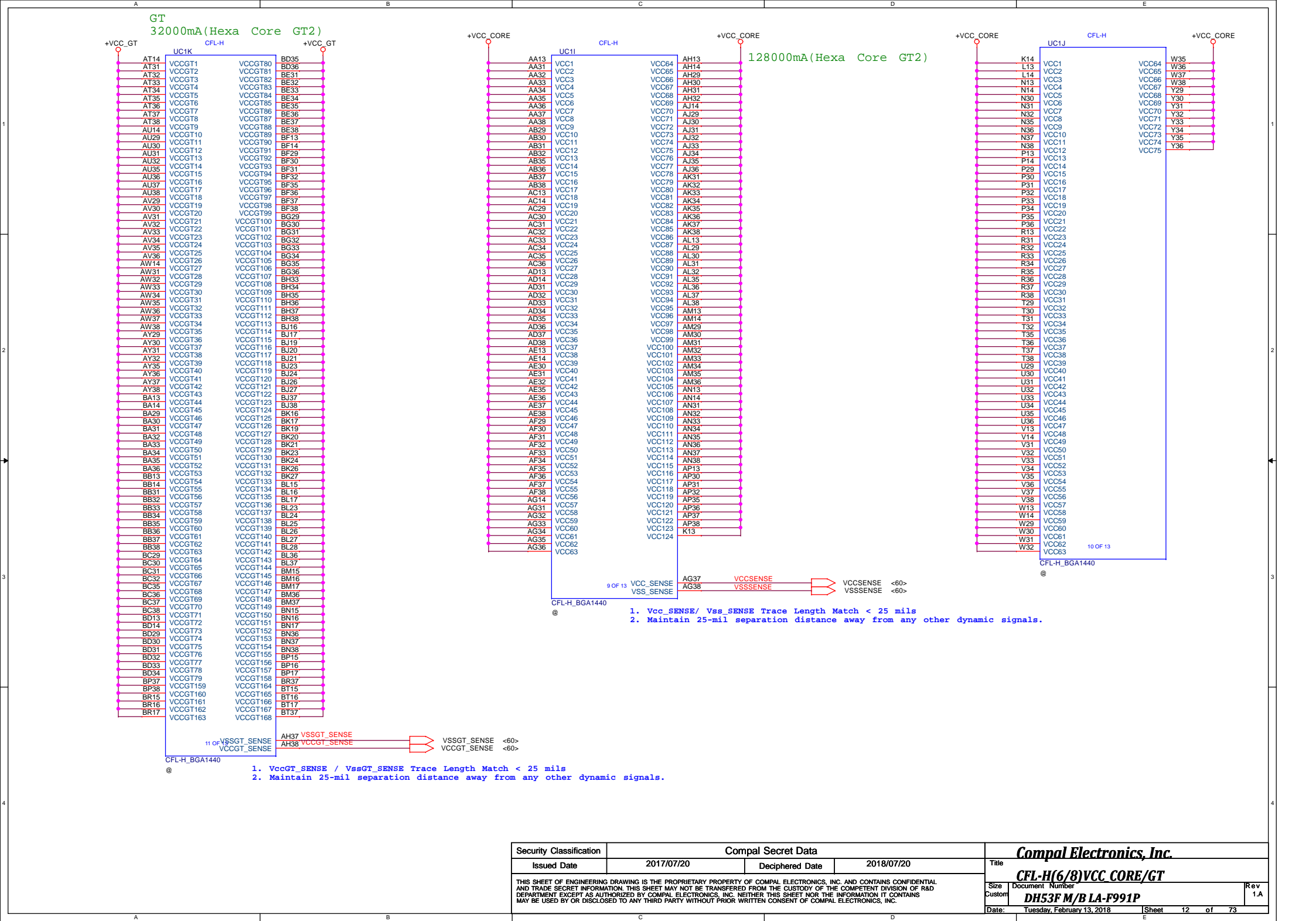
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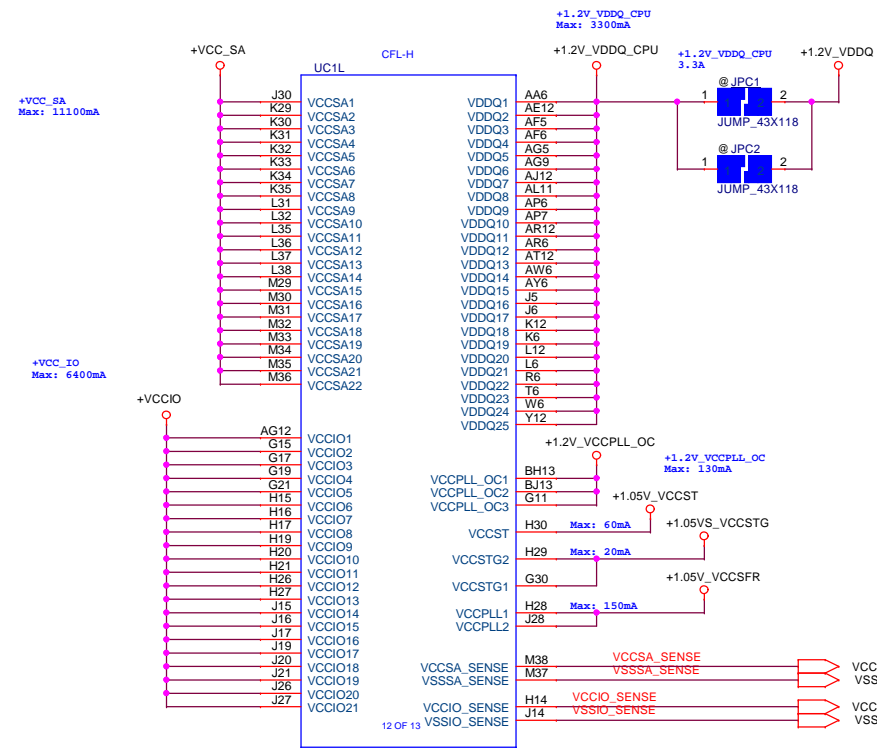


571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

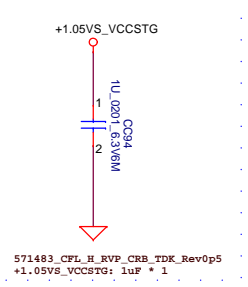
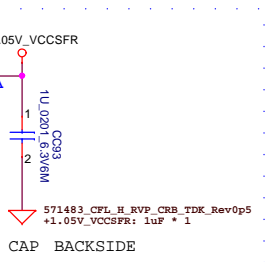
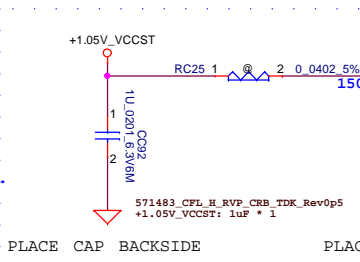
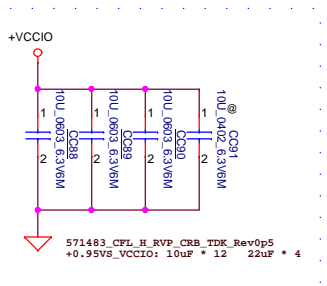
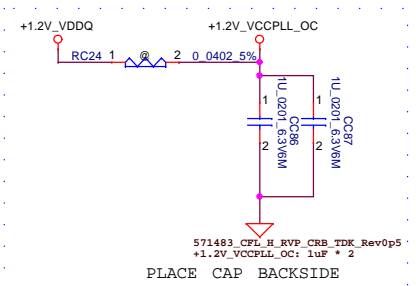
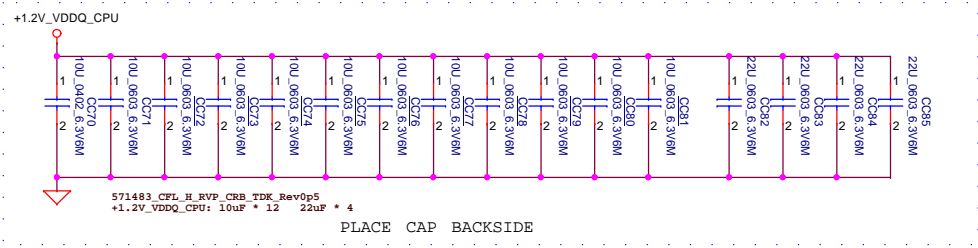


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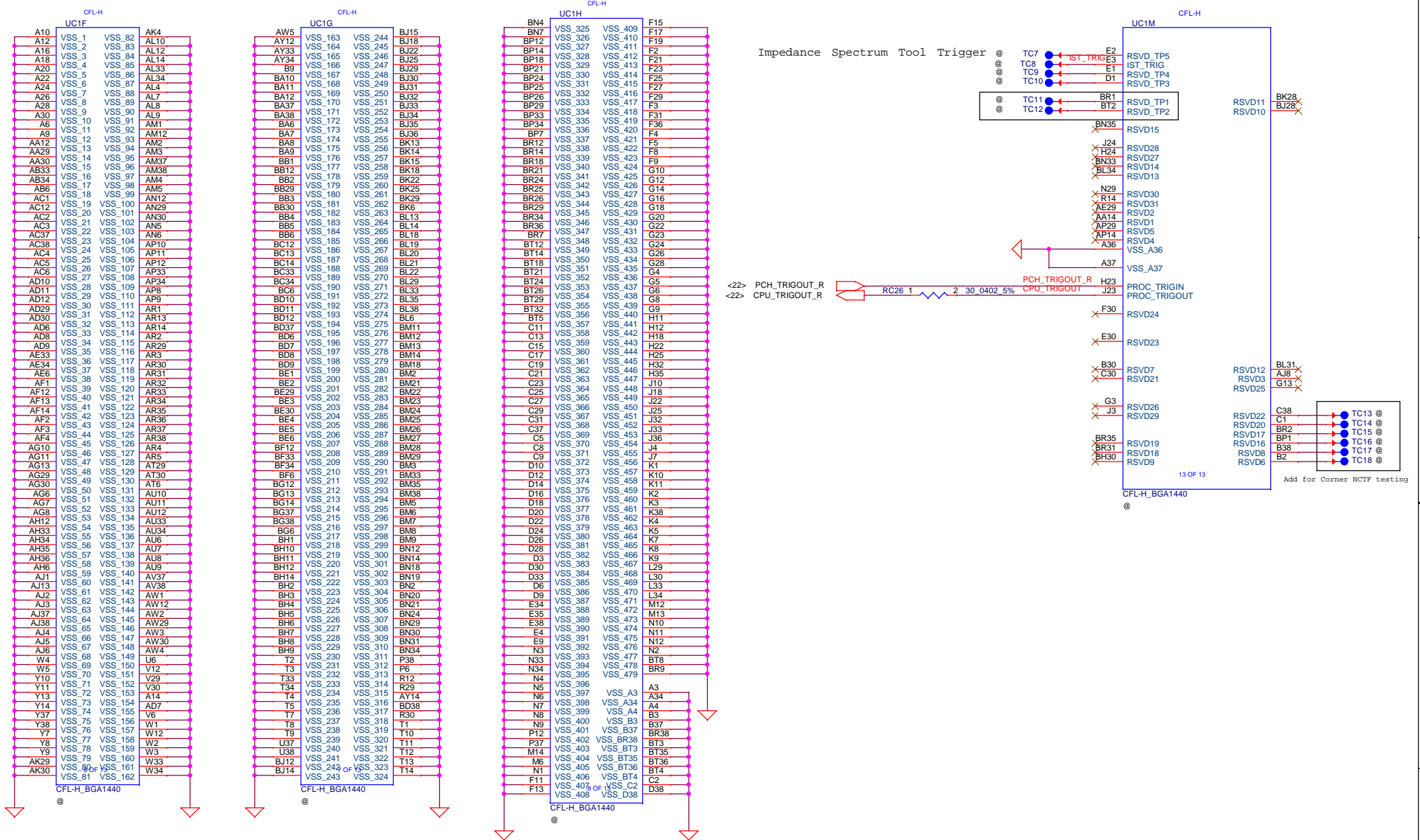


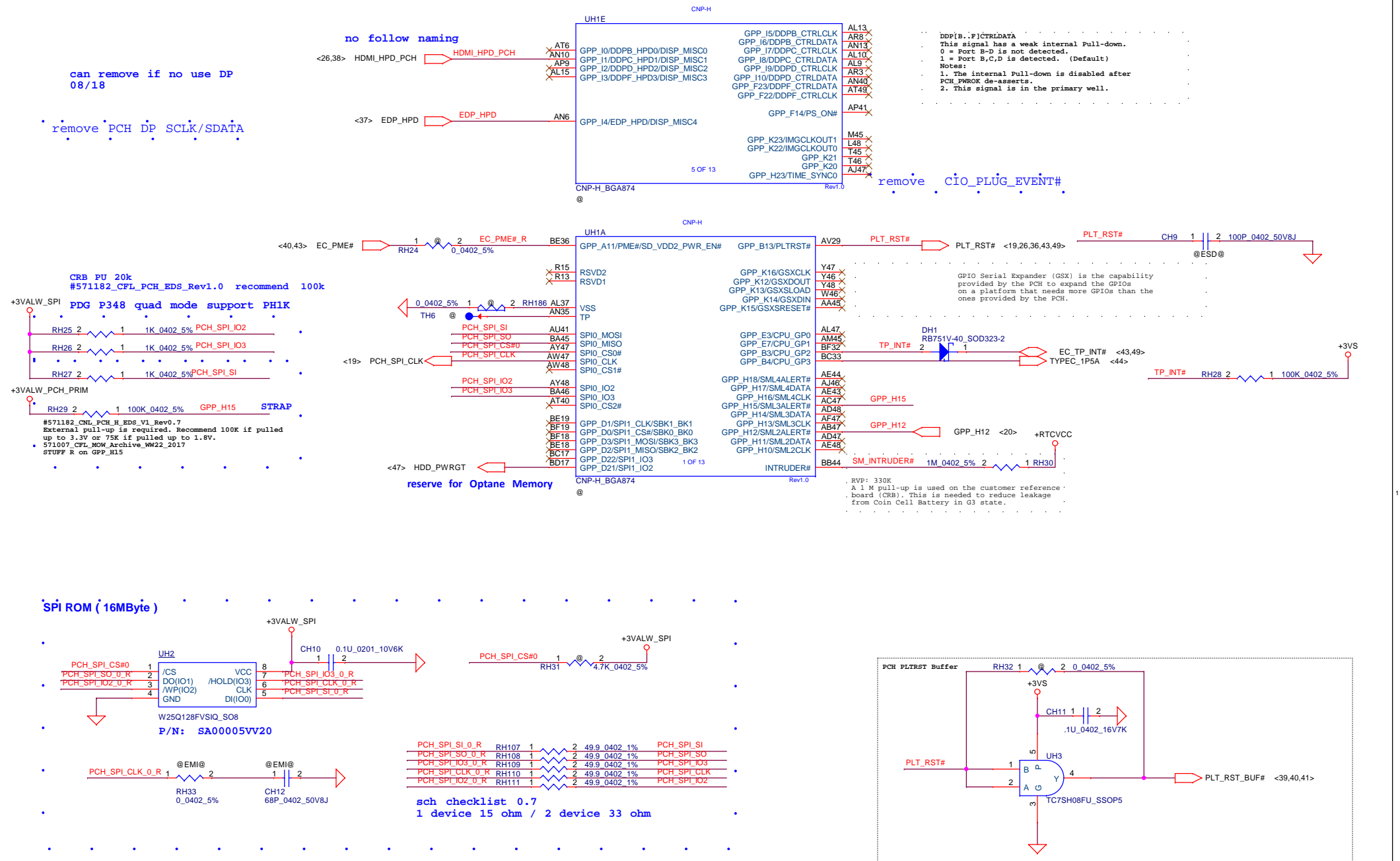


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

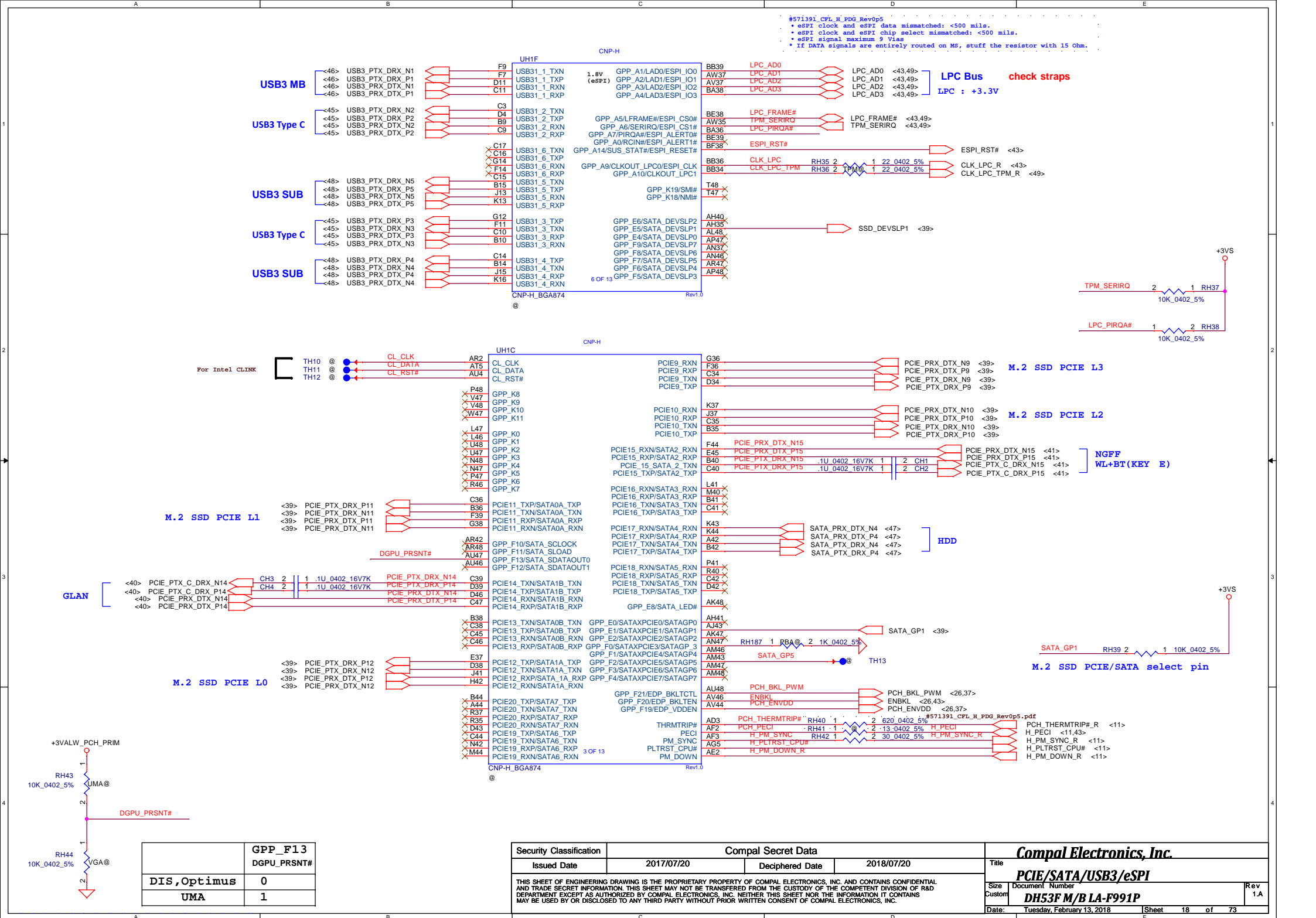


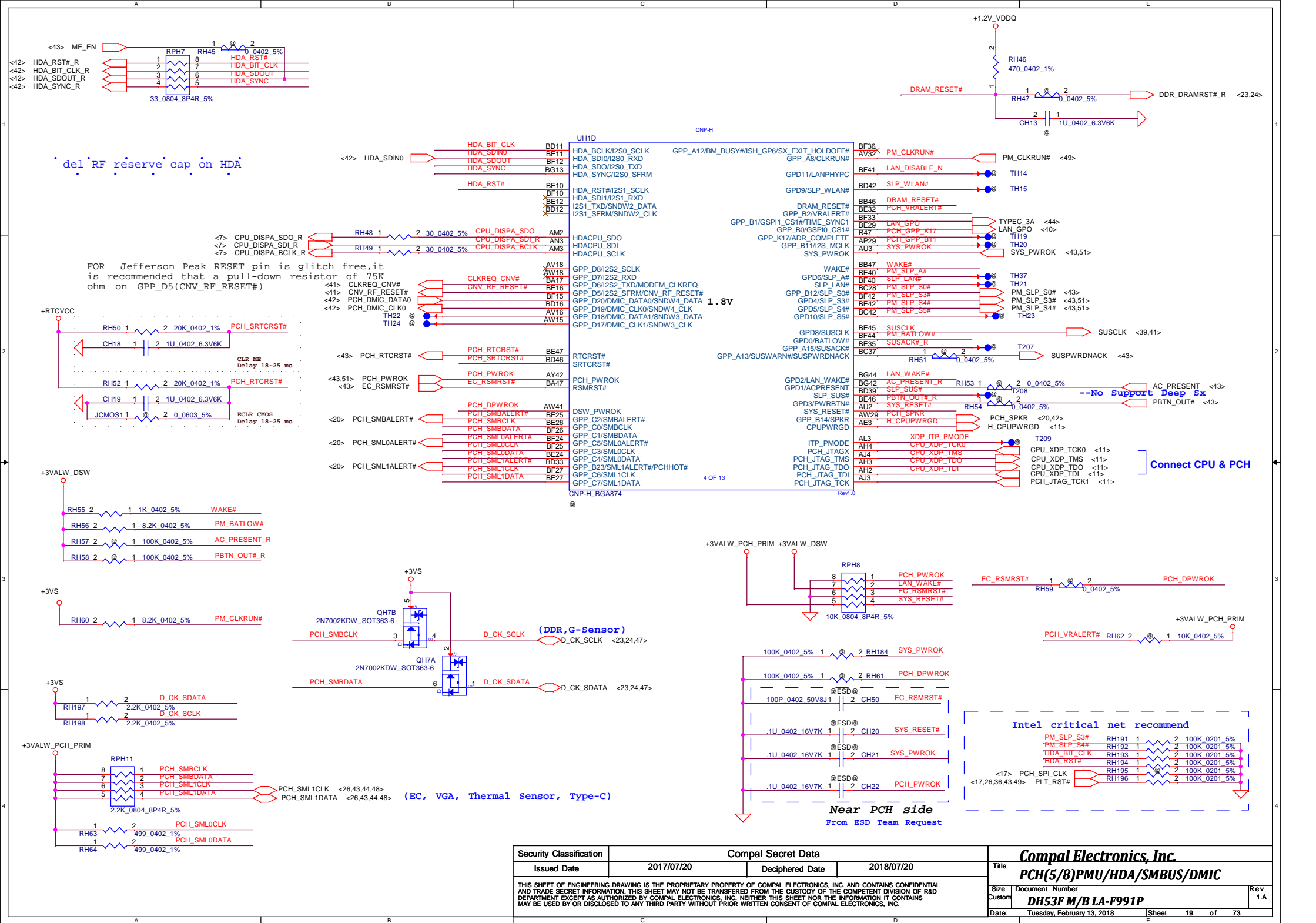
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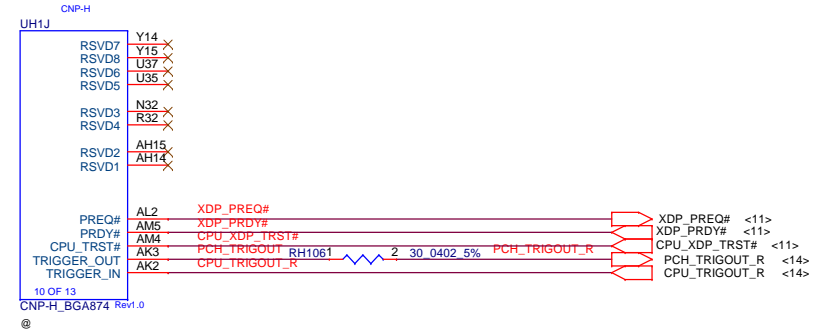
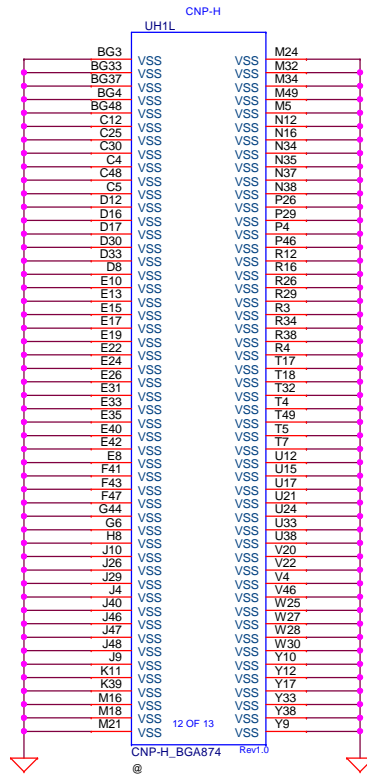
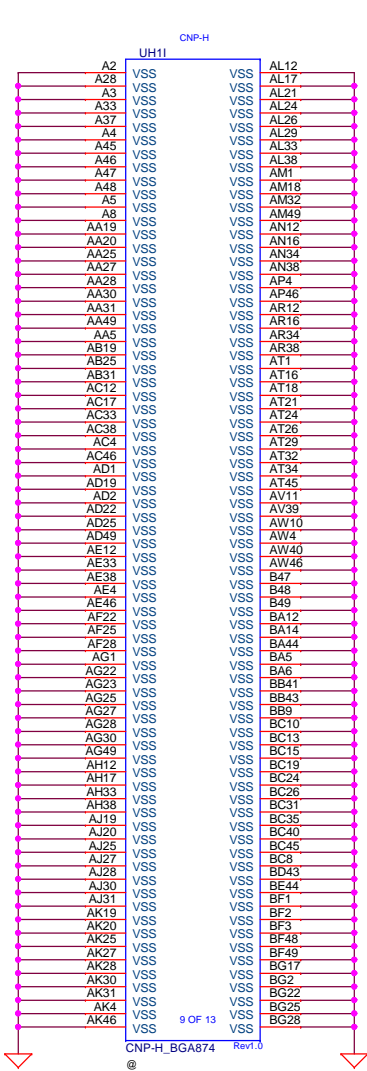




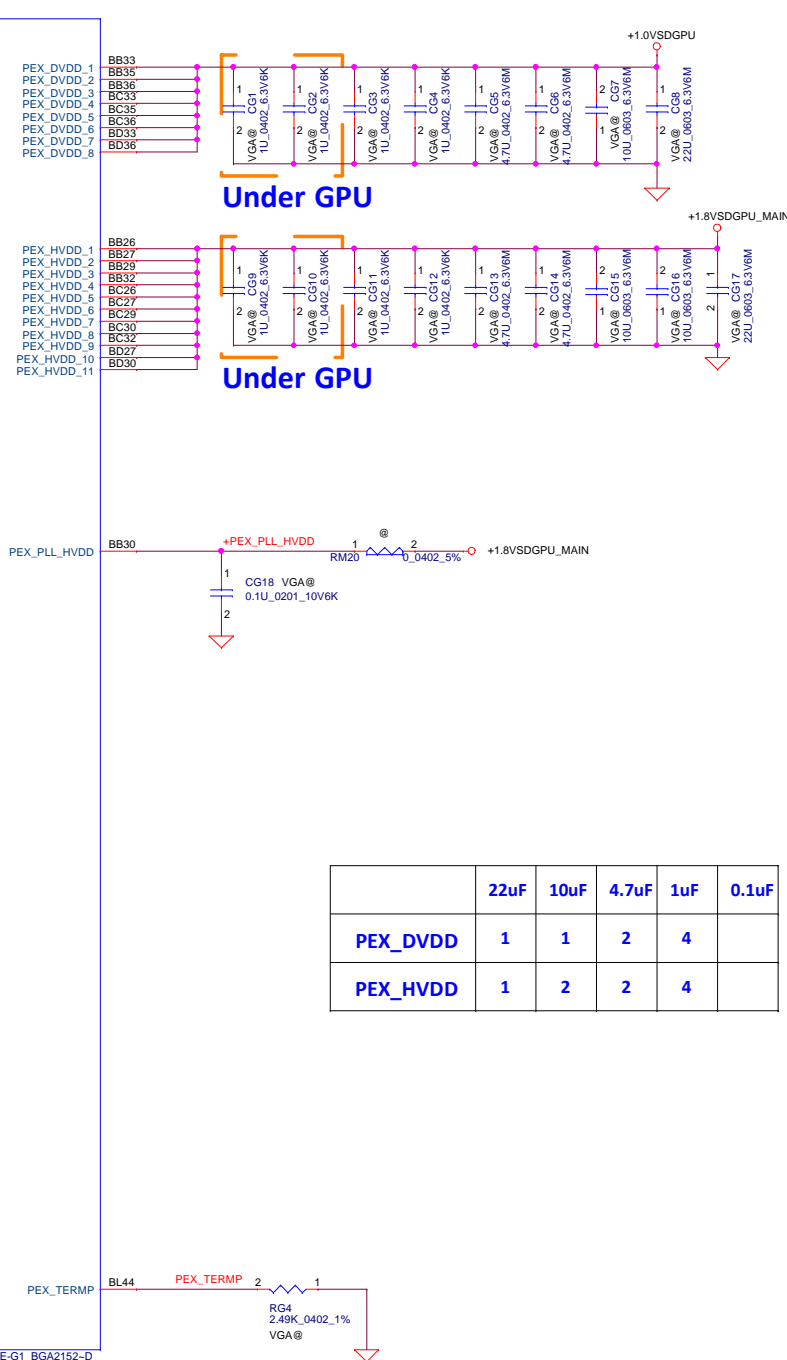
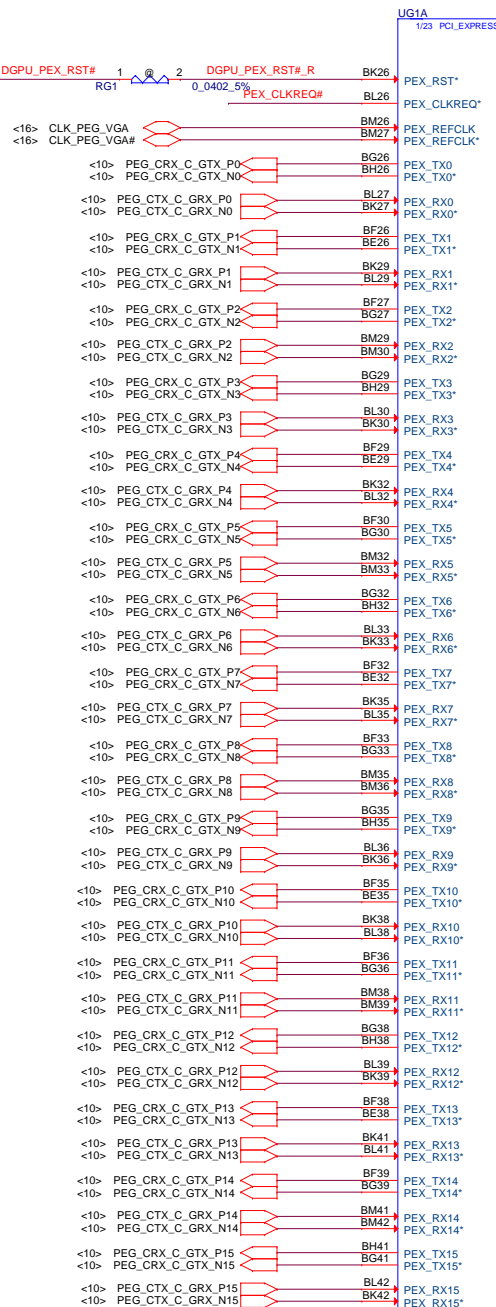
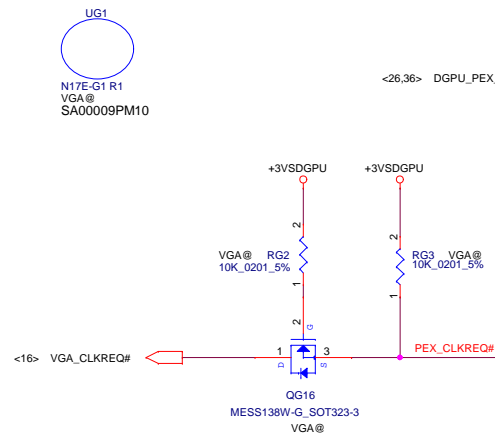
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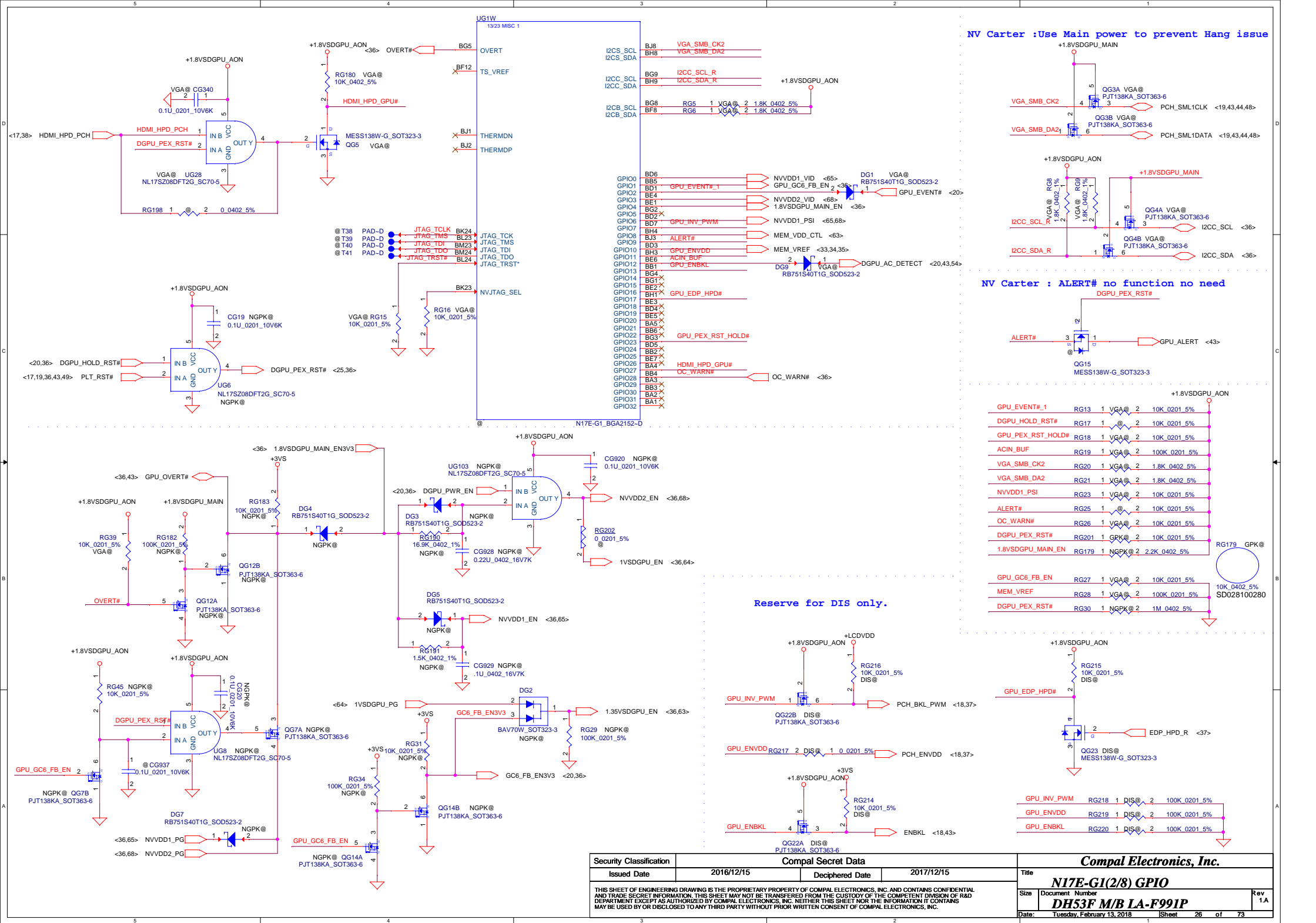


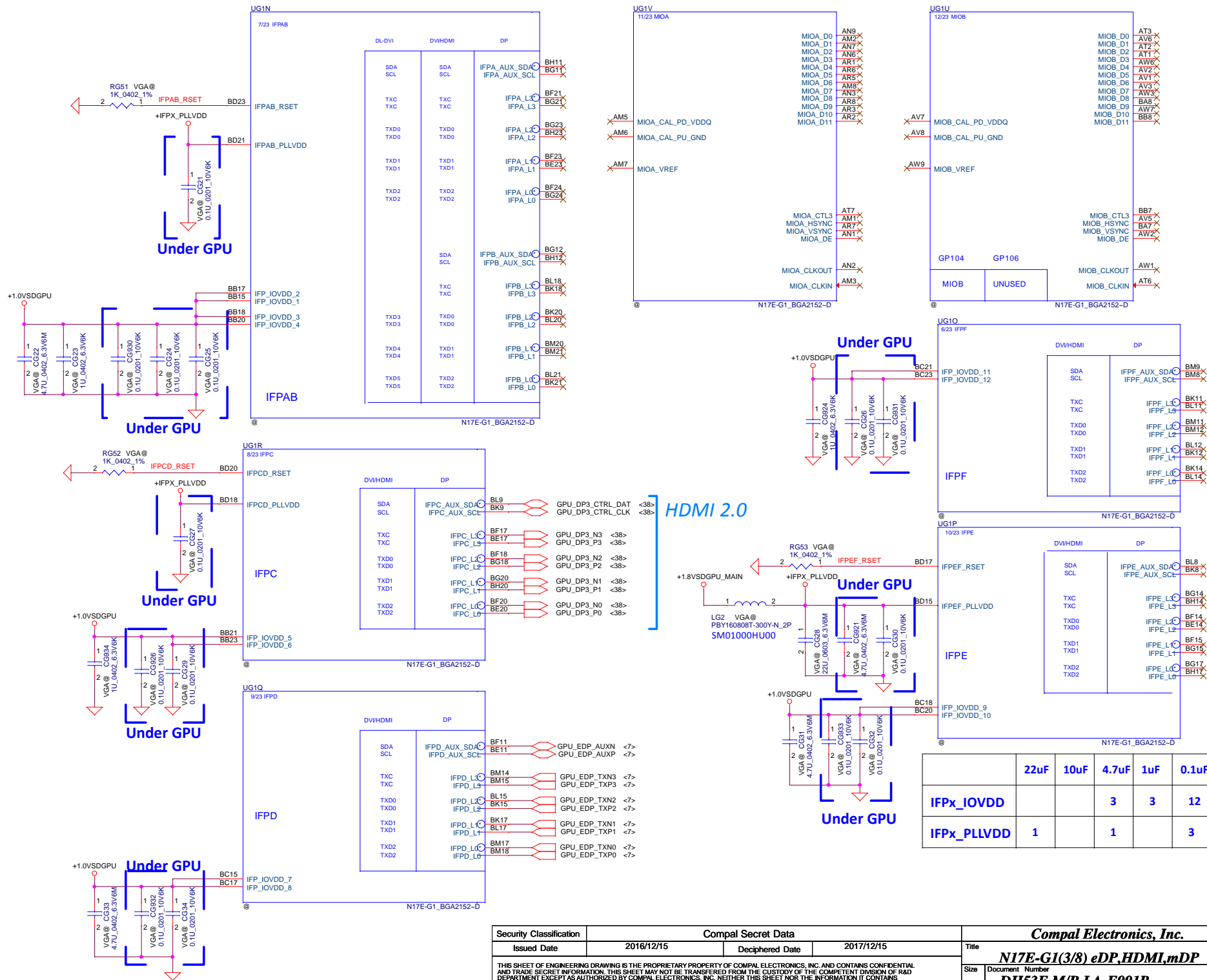


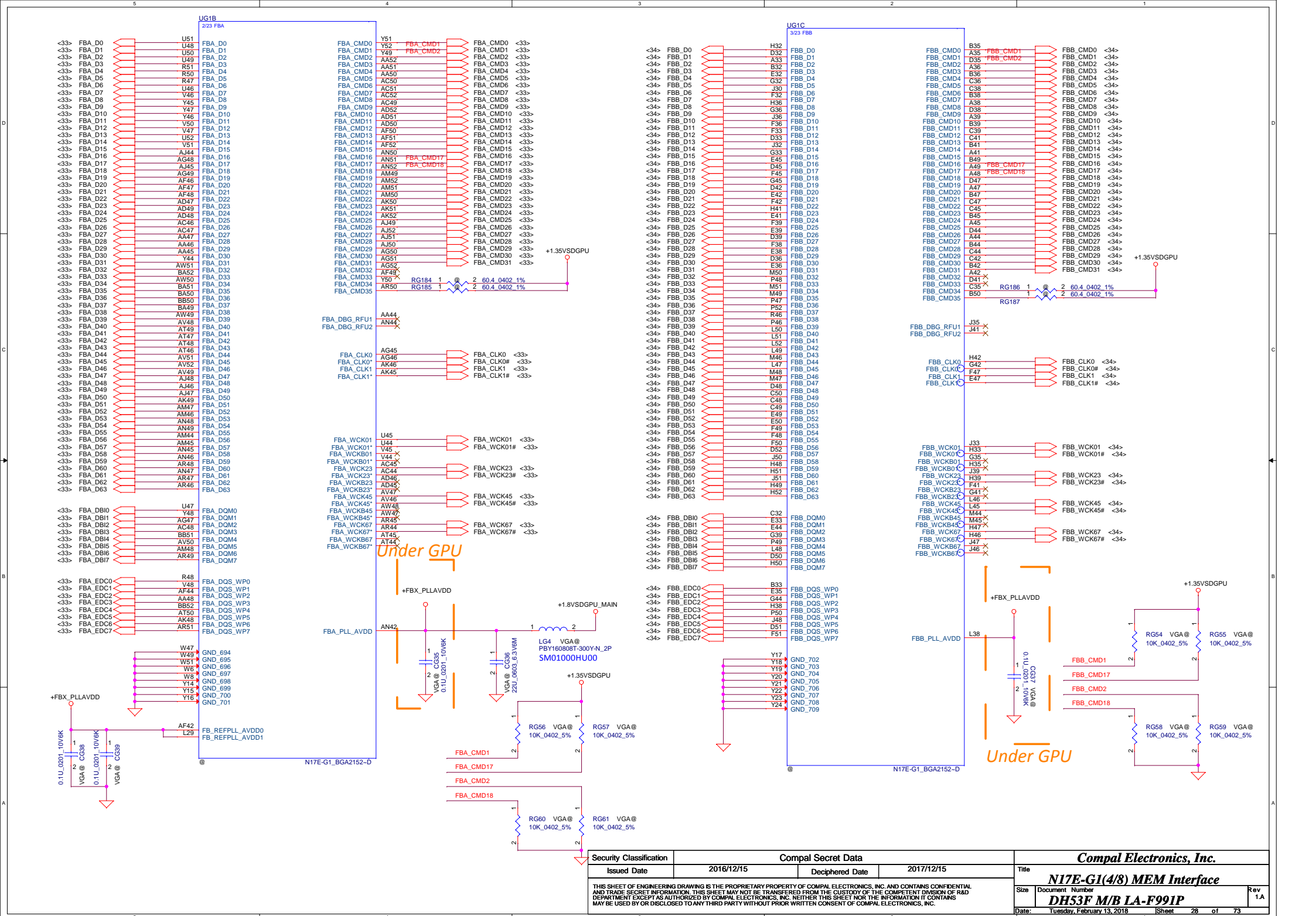
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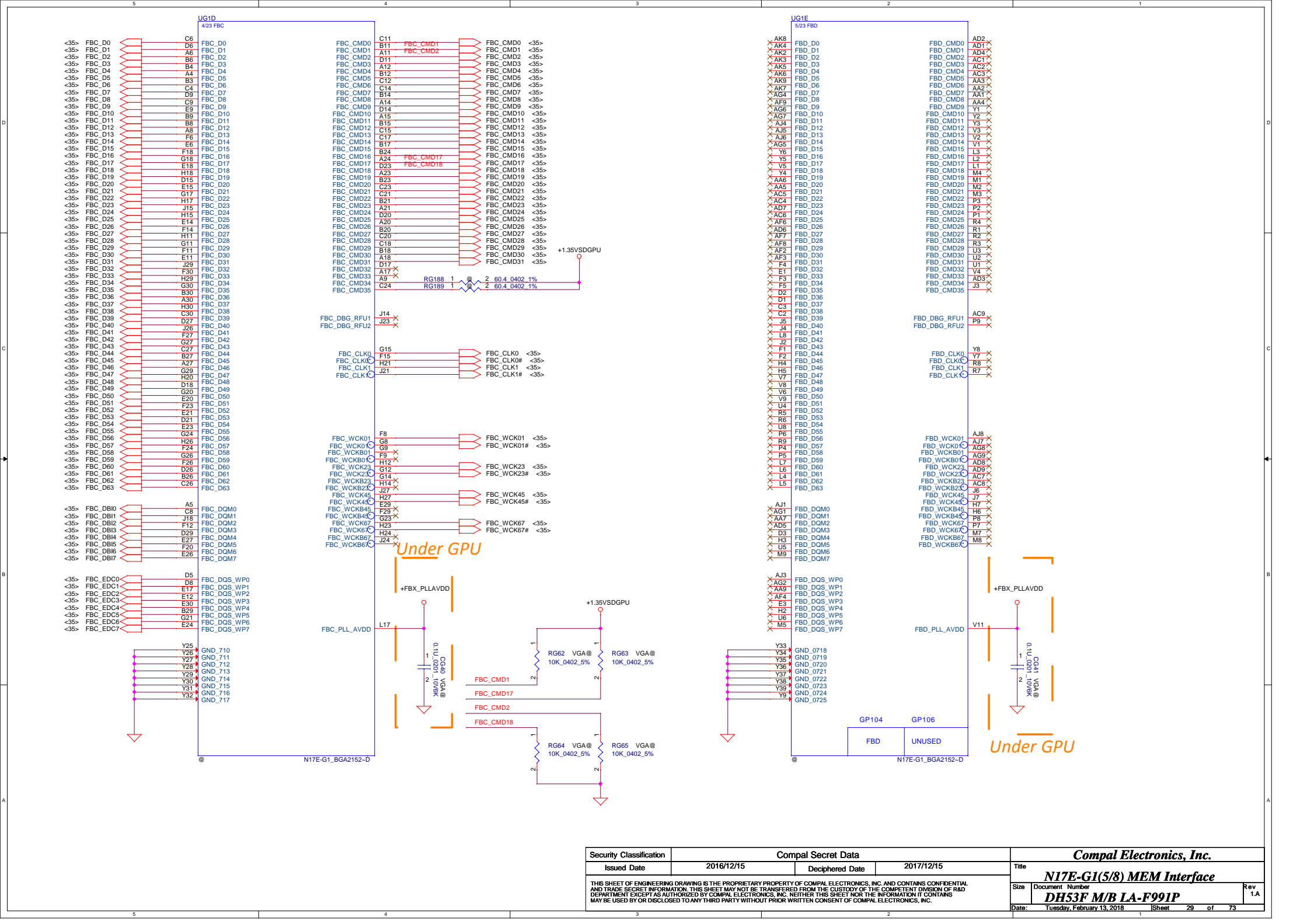


| | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|----------|------|------|-------|-----|-------|
| PEX_DVDD | 1 | 1 | 2 | 4 | |
| PEX_HVDD | 1 | 2 | 2 | 4 | |









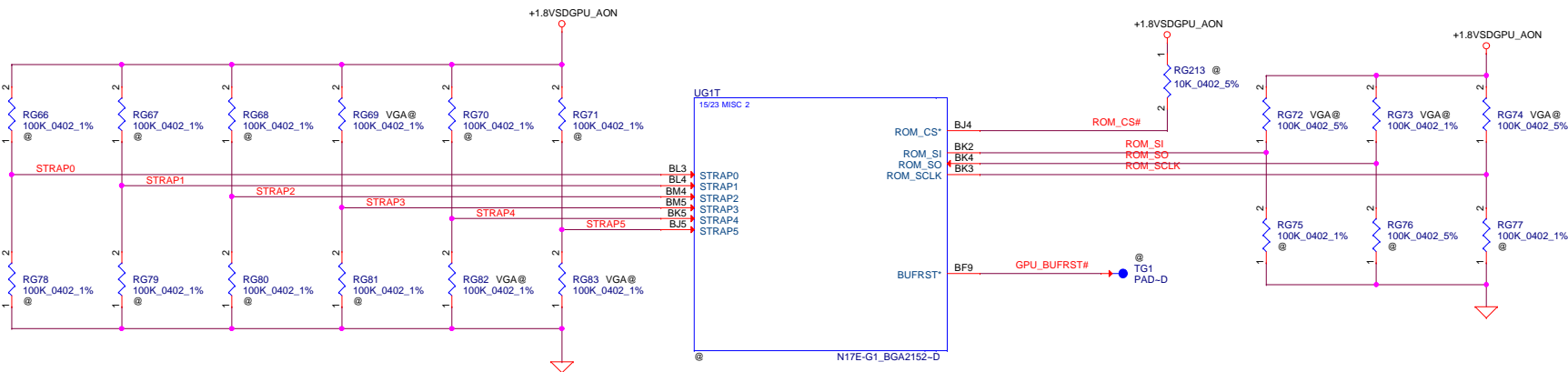


Table 2. N17E-G1 GDDR5 Recommended Memories

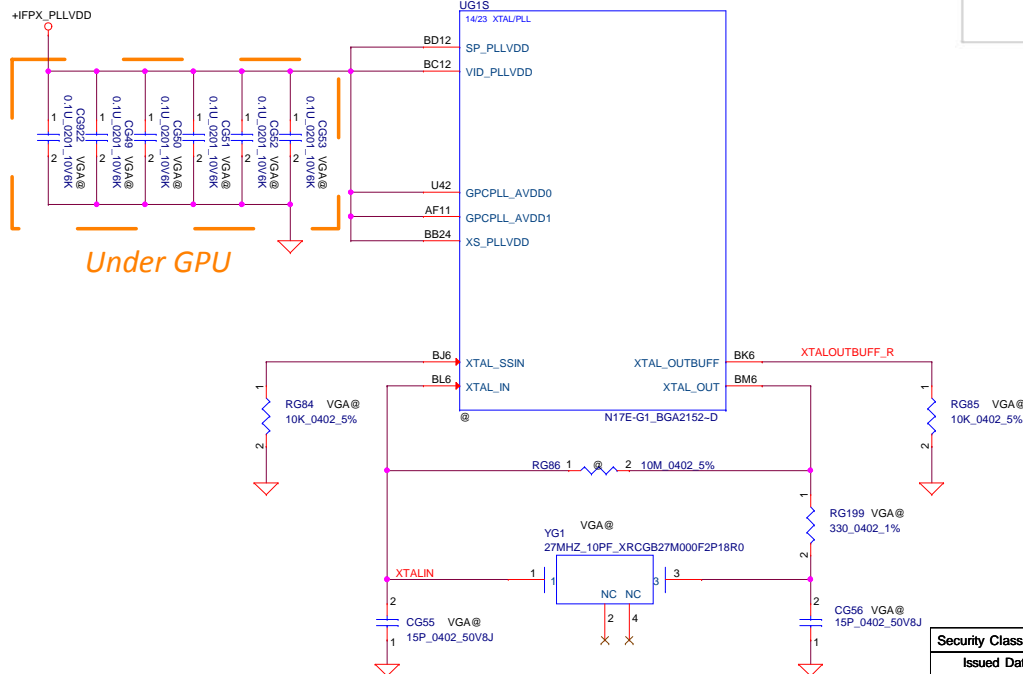
| Memory Density | Allowed Memory Configuration | FBVDD/Q | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert | Qual Plan | Status |
|----------------|------------------------------|------------------------------|---------|--------------------------|--------------|-------|--------------------|-----------------|-----------|-----------------------|
| 8 Gb | 256Mx32 | 1.35V and 1.55V ² | Samsung | K4G80325F8-HC25 | B-die | 0x0 | 8 Gbps | N/A | Full | Production ready |
| | | 1.35V and 1.5V ² | Micron | MT51J256M32HF-80:A | A-die | 0x1 | 8 Gbps | N/A | Full | Production ready |
| | | 1.35V and 1.55V ² | Hynix | H5GQ8H24MJR-R4C | M-die | 0x2 | 8 Gbps | N/A | Full | Post production ready |
| 4 Gb | 128Mx32 | 1.35V and 1.55V ² | Samsung | K4G41325FE-HC25 | E-die | 0x7 | 8 Gbps | N/A | Full | Post production ready |
| | | 1.35V and 1.55V ² | Hynix | H5GQ4H24AJR-R4C | A-die | 0x6 | 8 Gbps | N/A | Full | Post production ready |

Notes:

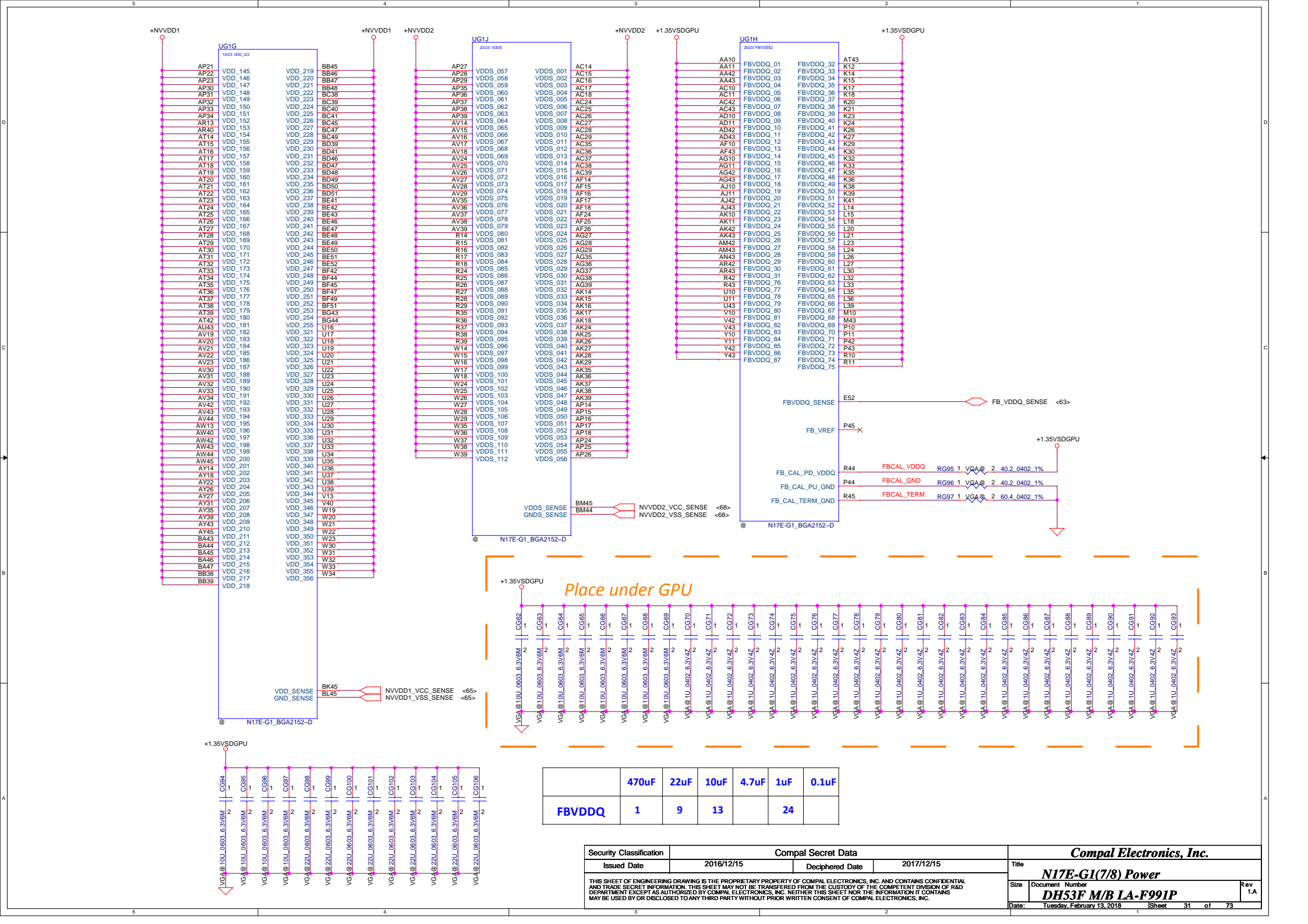
- For N17E-G1, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
- N17E-G1 runs WCLK up to 3000 MHz with FBVDD = 1.35V. DV5 is required to run WCLK > 3000 MHz.

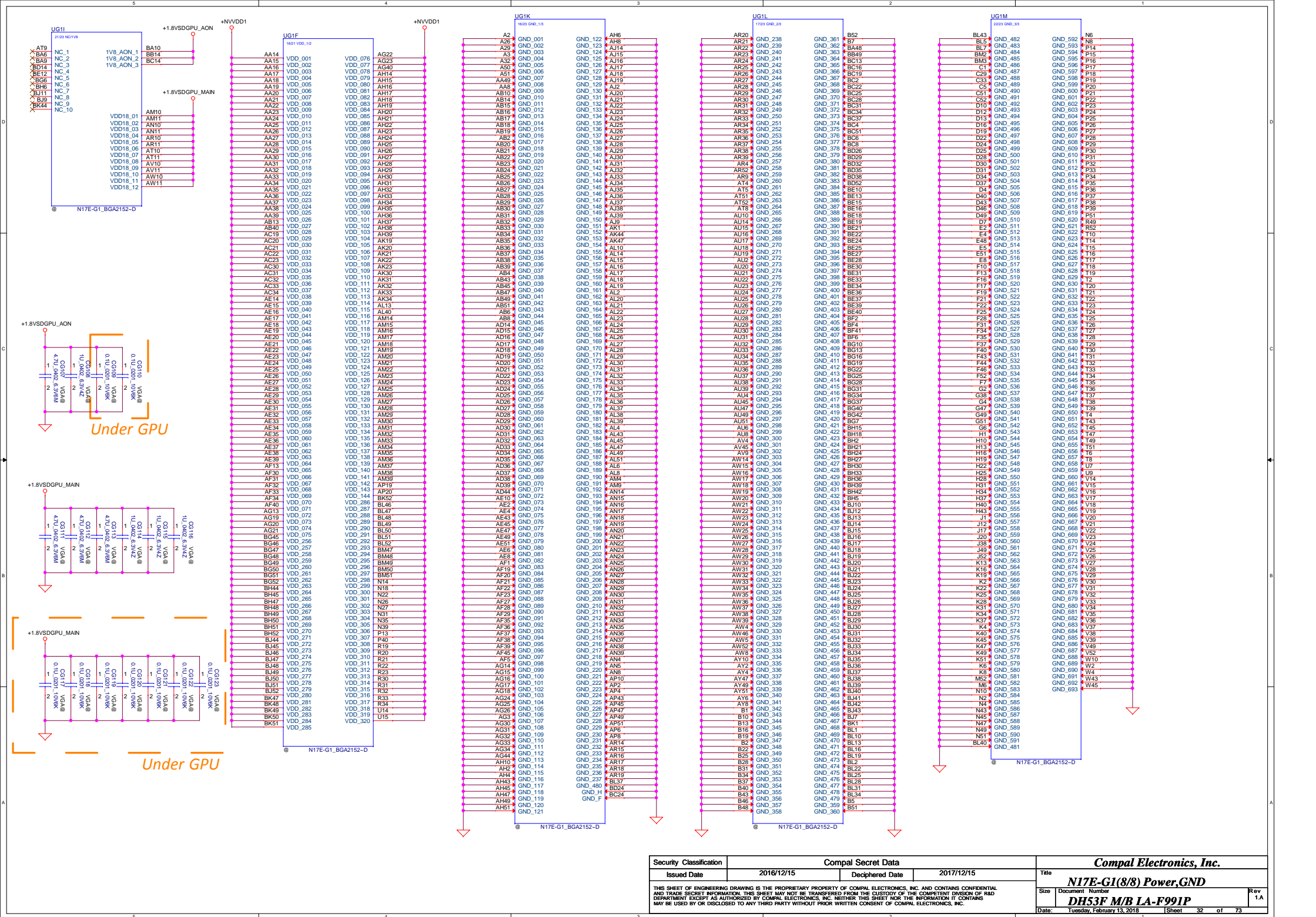
Table 5.3 RAMCFG

| Strap Pins see Note | | | RAMCFG Setting Number | |
|---------------------|--------|--------|--|--|
| STRAP2 | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers) | |
| L | L | L | 0 (0x0000) | |
| L | L | H | 1 (0x0001) | |
| L | H | L | 2 (0x0002) | |
| L | H | H | 3 (0x0003) | |
| H | L | L | 4 (0x0004) | |
| H | L | H | 5 (0x0005) | |
| H | H | L | 6 (0x0006) | |
| H | H | H | 7 (0x0007) | |



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GDDR5_C

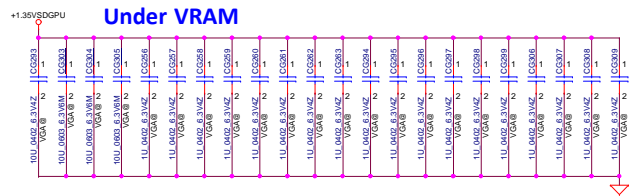
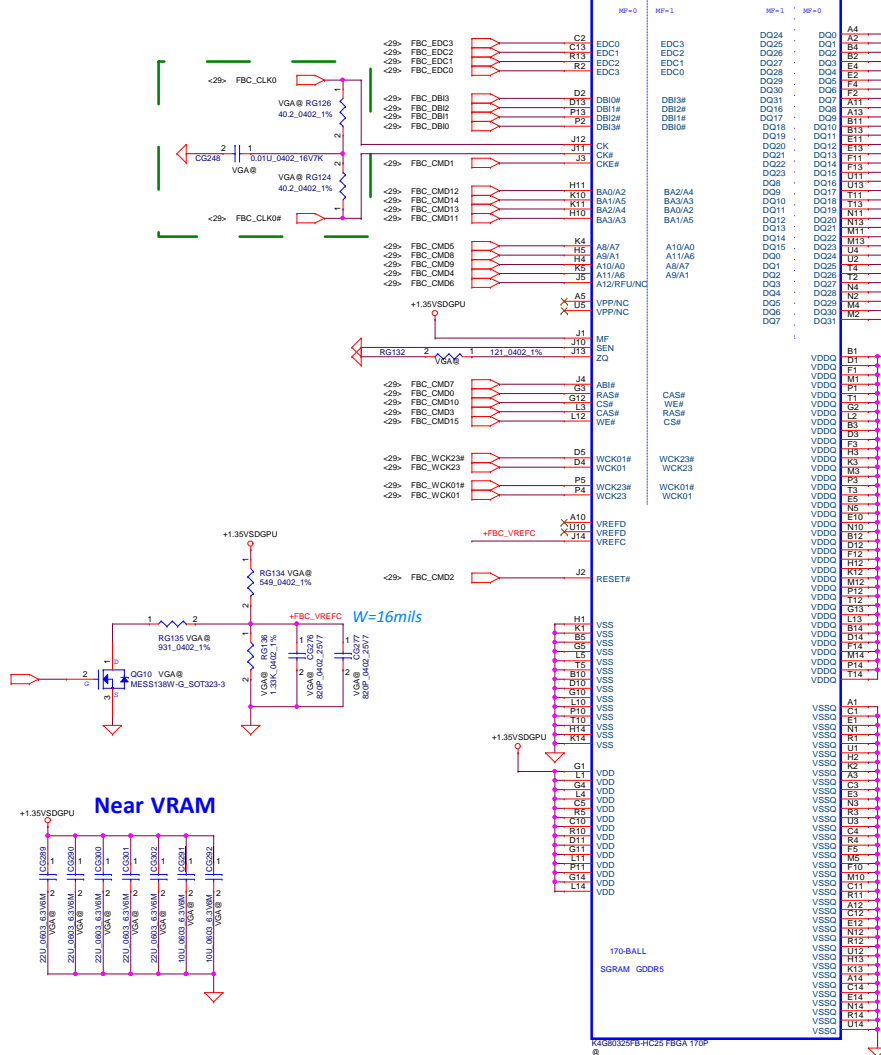
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MF=0

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B

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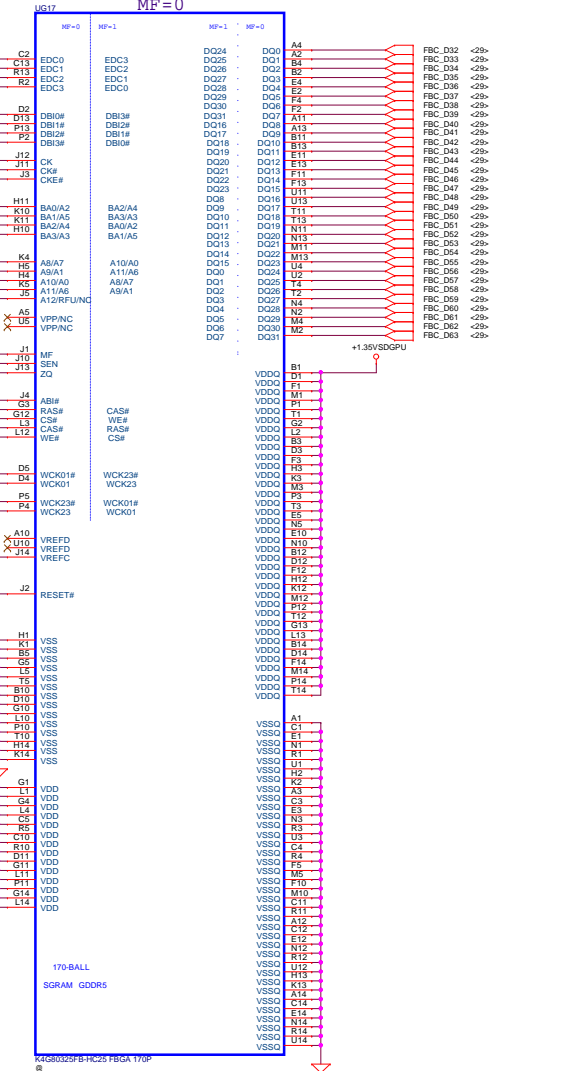
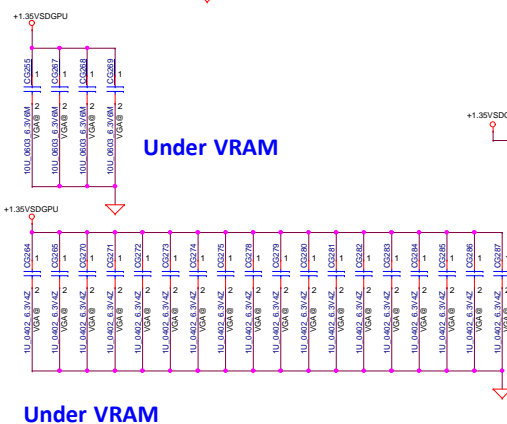


Under VRAM
18 x 1uF (0402 X65)
4 x 10uF (0402 X65)

Near VRAM
2 x 10uF (0402 X65) 2 GND/PWR vias for each cap.
5 x 22uF (0603 X65) 2 GND/PWR vias for each cap

Near VRAM

Under VRAM



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| | | | | Rev | 1A |
| | | | | DH53F M/B LA-F991P | |
| | | | | Tuesday, February 13, 2018 | |
| | | | | Sheet 35 of 73 | |

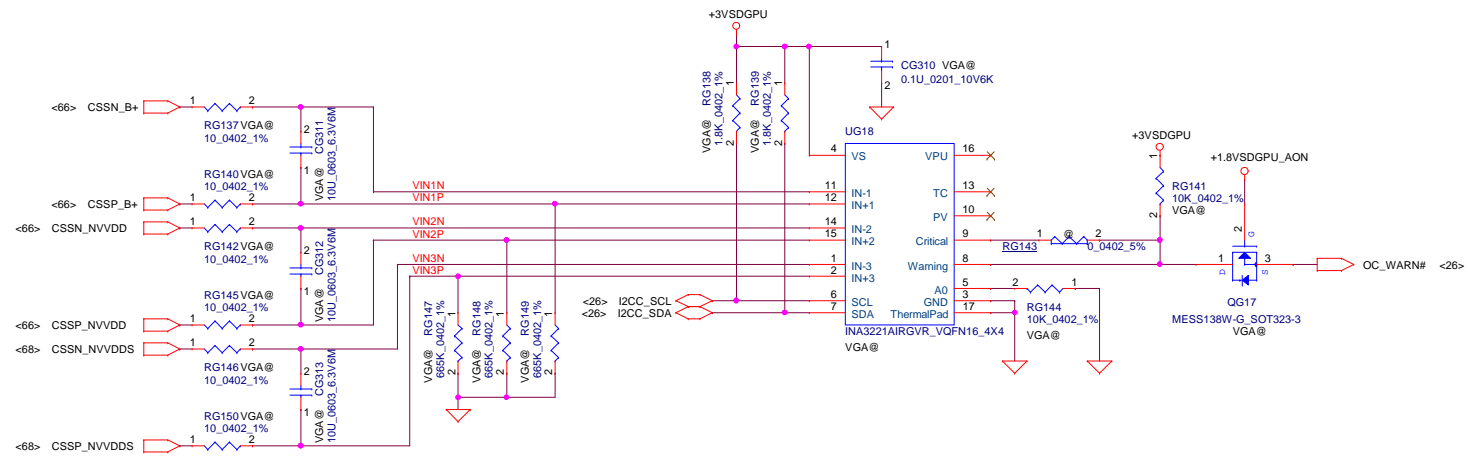
Compal Electronics, Inc.

N17E-GDDR5_C

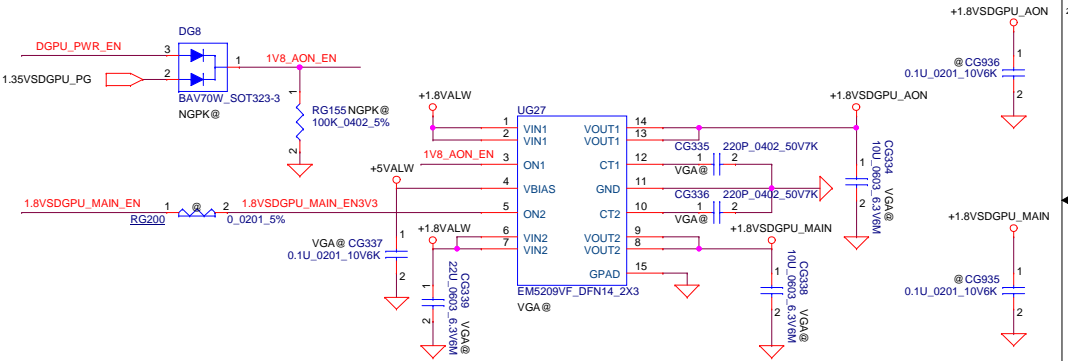
DH53F M/B LA-F991P

Tuesday, February 13, 2018

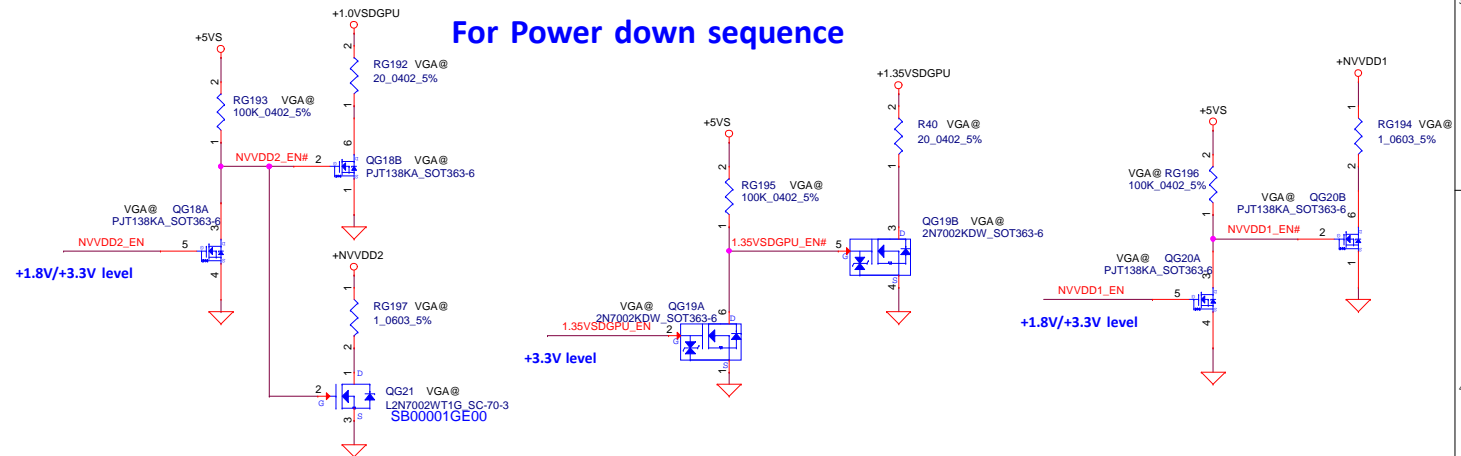
Sheet 35 of 73



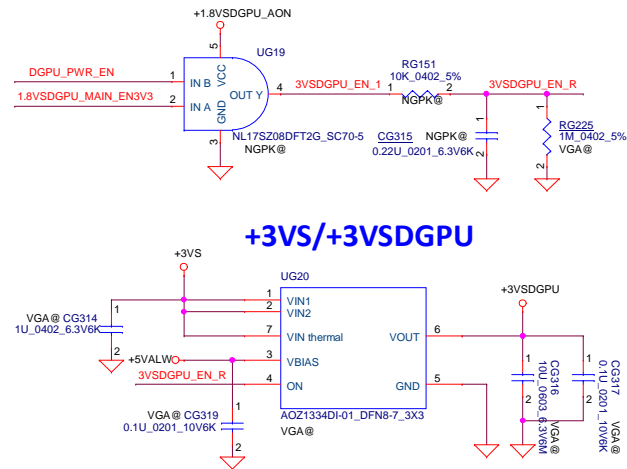
+1.8VALW to +1.8VSDGPU_AON & +1.8VSDGPU_MAIN



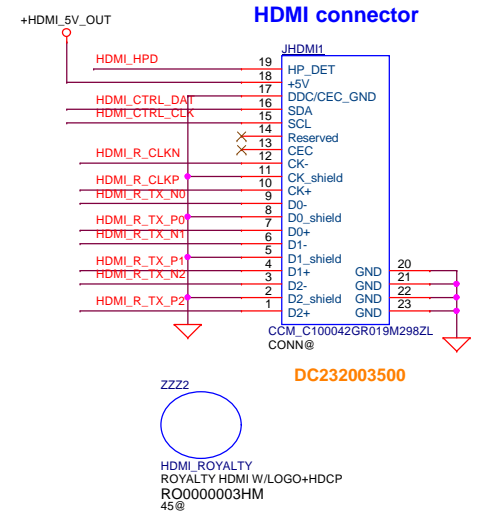
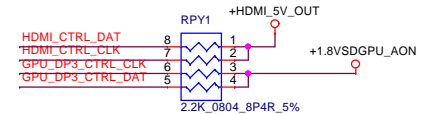
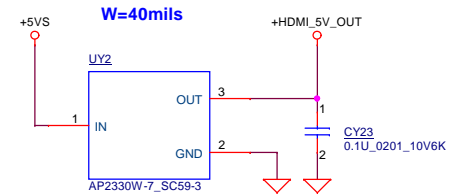
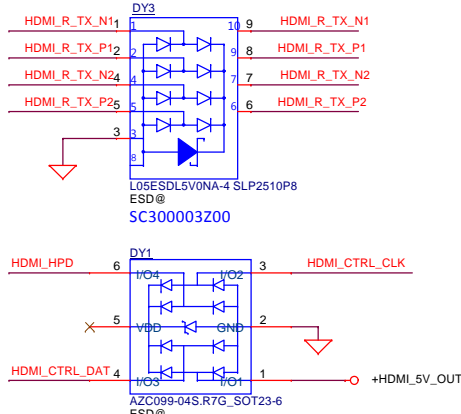
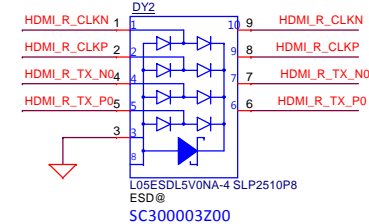
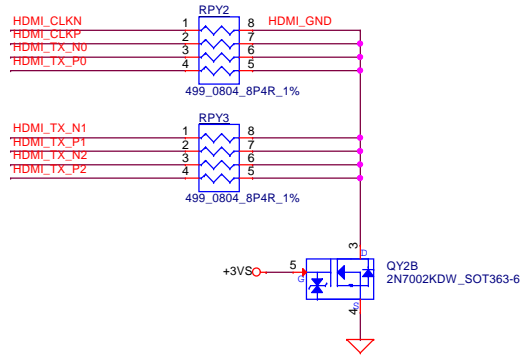
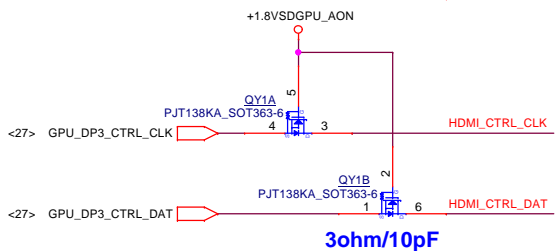
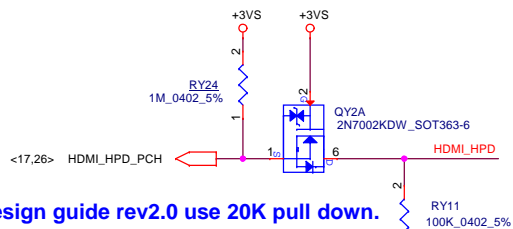
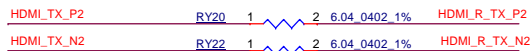
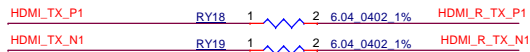
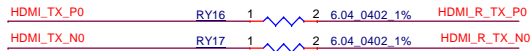
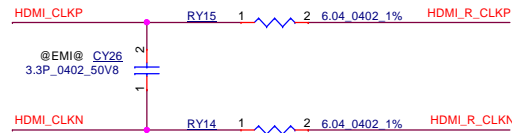
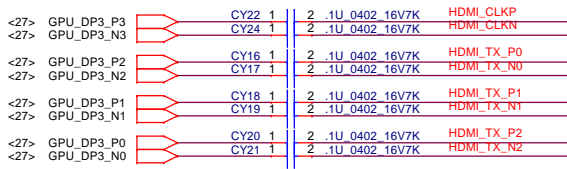
For Power down sequence



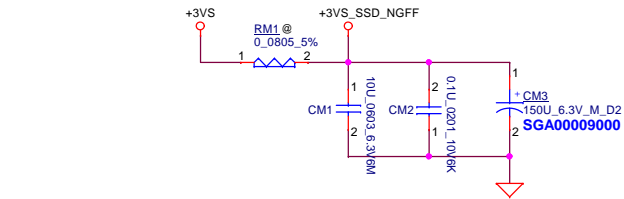
+3VS/+3VSDGPU



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| | | | | Size | Document Number |
| | | | | Date | Rev |
| | | | | Tuesday, February 13, 2016 | 1A |
| | | | | Sheet | of |
| | | | | 36 | 73 |



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| Size | Document Number | Rev | | 1.A | |
| Custom | DH53F M/B LA-F991P | | | | |
| Date: | Tuesday, February 13, 2018 | Sheet | 38 | of | 73 |



M.2 SSD

<18> PCIE_PRX_DTX_N9
<18> PCIE_PRX_DTX_P9
<18> PCIE_PTX_DRX_N9
<18> PCIE_PTX_DRX_P9

CM6 1 2 0.22U 0402 16V7K
CM4 1 2 0.22U 0402 16V7K

PCIE_PTX_C_DRX_N9
PCIE_PTX_C_DRX_P9

<18> PCIE_PRX_DTX_N10
<18> PCIE_PRX_DTX_P10
<18> PCIE_PTX_DRX_N10
<18> PCIE_PTX_DRX_P10

CM5 1 2 0.22U 0402 16V7K
CM7 1 2 0.22U 0402 16V7K

PCIE_PTX_C_DRX_N10
PCIE_PTX_C_DRX_P10

<18> PCIE_PRX_DTX_N11
<18> PCIE_PRX_DTX_P11
<18> PCIE_PTX_DRX_N11
<18> PCIE_PTX_DRX_P11

CM8 1 2 0.22U 0402 16V7K
CM9 1 2 0.22U 0402 16V7K

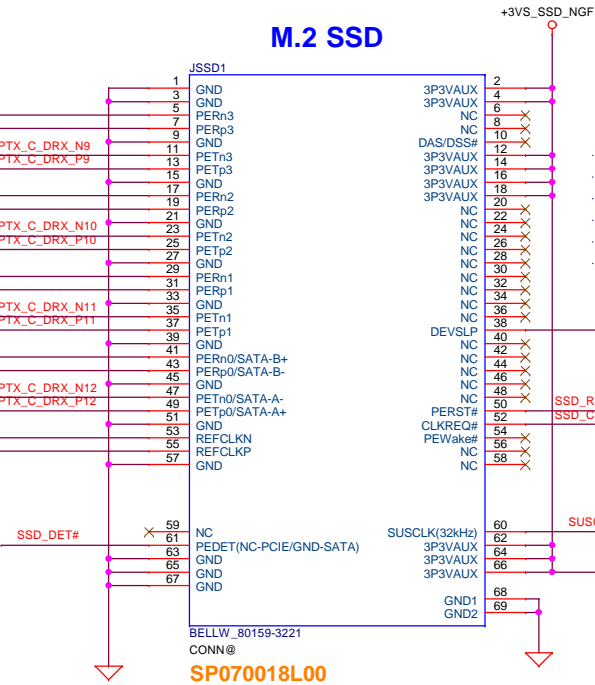
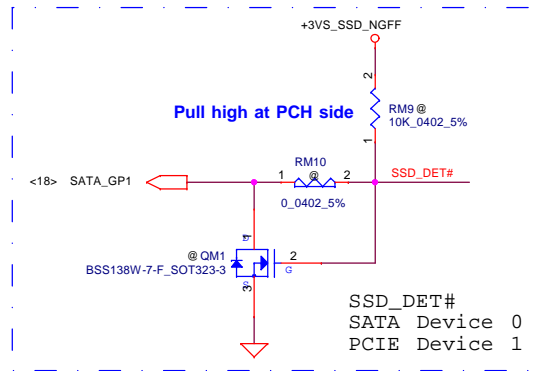
PCIE_PTX_C_DRX_N11
PCIE_PTX_C_DRX_P11

<18> PCIE_PRX_DTX_P12
<18> PCIE_PTX_DRX_N12
<18> PCIE_PTX_DRX_P12

CM10 1 2 0.22U 0402 16V7K
CM11 1 2 0.22U 0402 16V7K

PCIE_PTX_C_DRX_N12
PCIE_PTX_C_DRX_P12

<16> CLK_PCIE_NGFF#
<16> CLK_PCIE_NGFF



SSD_RST#_R
Place close to JSSD pin 50
ESD request to reserve.

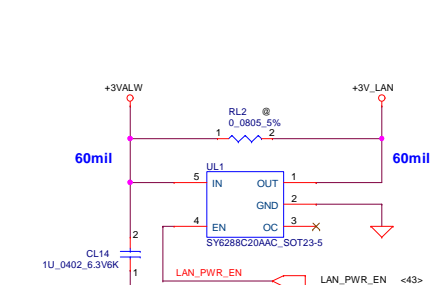
SSD_DEVSLP1
SSD_RST#_R
SSD_CLKREQ#_R
PLT_RST_BUF#
SSD_CLKREQ#

SUSCLK_SSD
SUSCLK

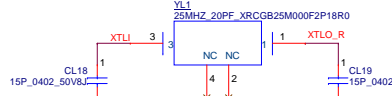
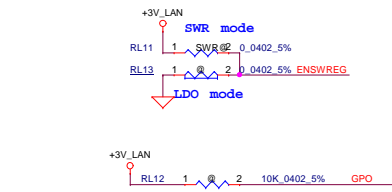
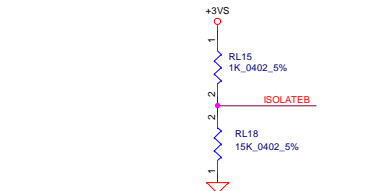
SSD_RST#_R
SSD_CLKREQ#_R
reserve for Optane Memory

| | | | | | |
|---|------------|--------------------|------------|--------------------------|----------------------------|
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| | | | | Date: | Tuesday, February 13, 2018 |
| | | | | Sheet | 39 of 73 |
| | | | | Rev | 1.A |

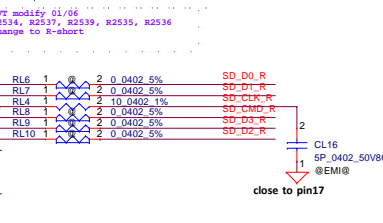
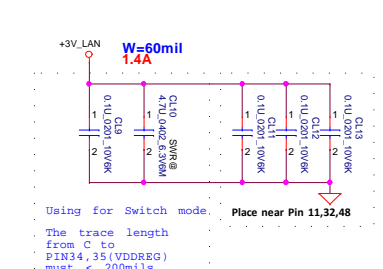
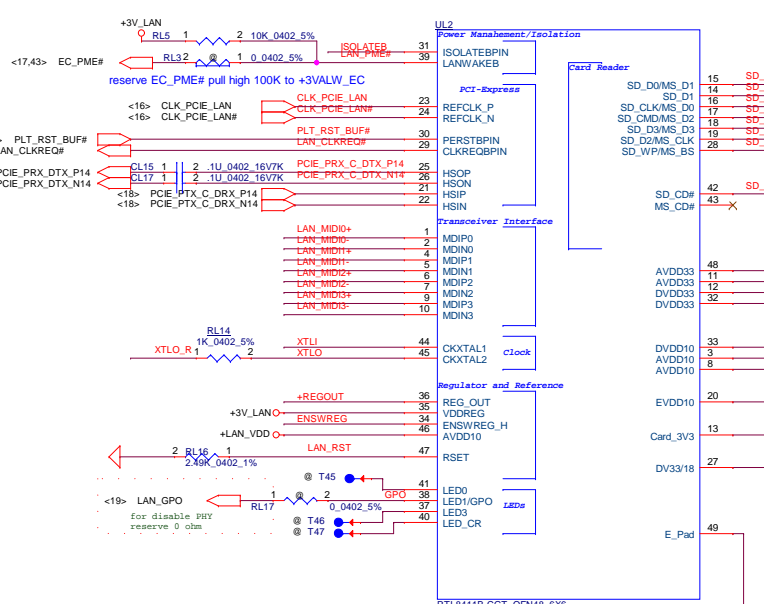
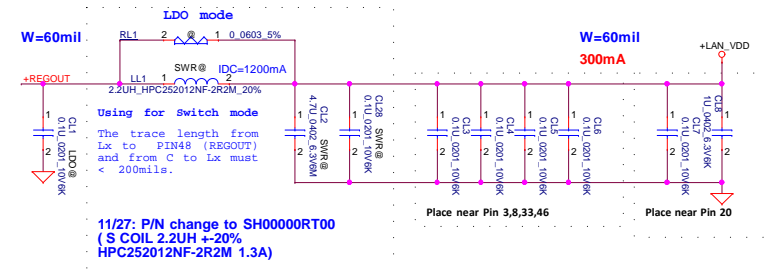
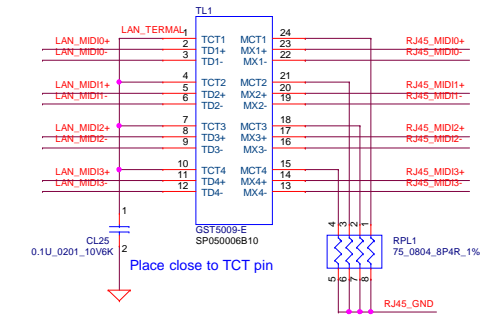
LAN-RTL8411B



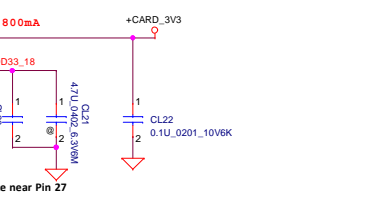
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms



P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



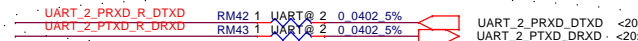
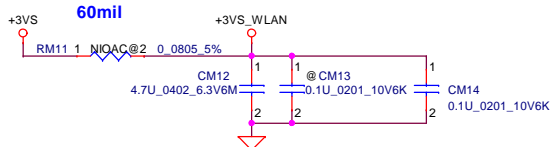
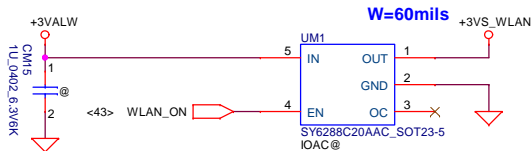
| | Protect contact | Card contact |
|----------------------|-----------------------|--------------|
| Write protect (Lock) | Write Enable (Unlock) | |
| Card Uninsert | Open | Open |
| Card insert | Open | Close |



| | Protect contact | Card contact |
|----------------------|-----------------------|--------------|
| Write protect (Lock) | Write Enable (Unlock) | |
| Card Uninsert | Open | Open |
| Card insert | Open | Close |

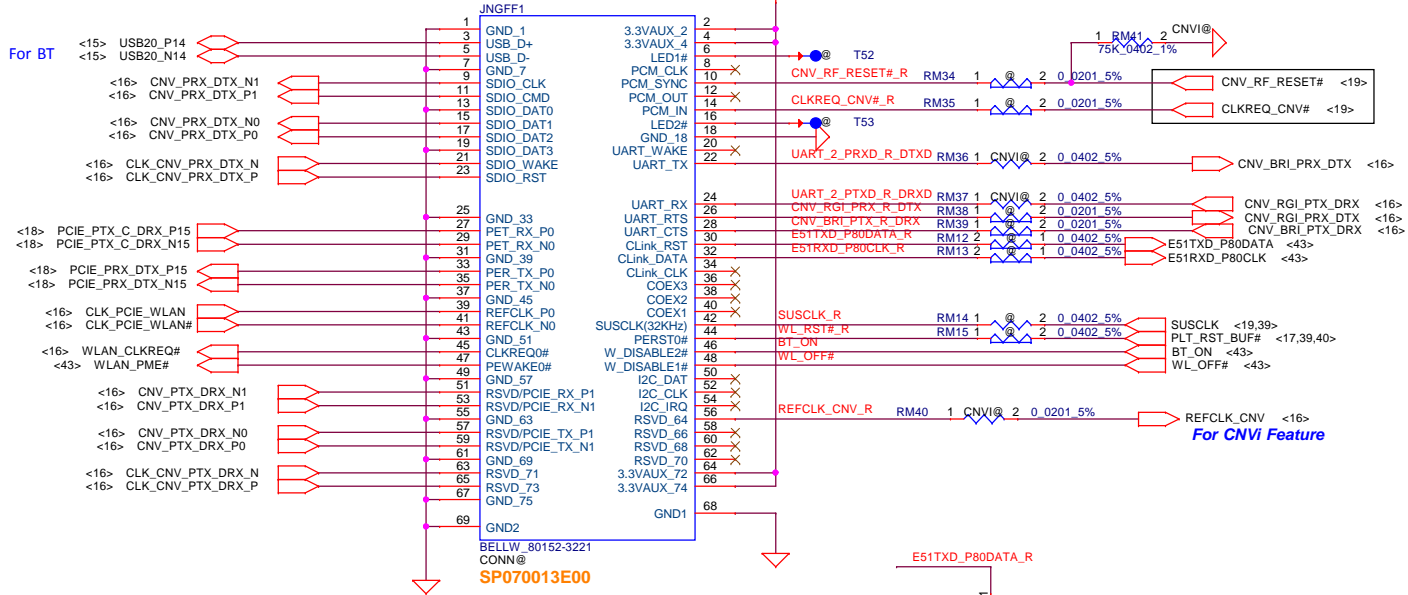


Wireless LAN



Co-layout with CNVi PH +3VS at SOC side, for win7 USB3 debug

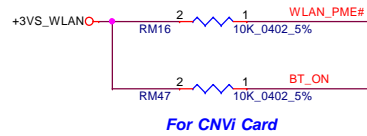
KEY E



NGFF WL+BT (KEY E)

| | | | |
|----|--------------------------------|---------------------|----|
| 74 | 3.3V | GND | 75 |
| 72 | 3.3V | RESERVED/REFCLKN1 | 73 |
| 70 | UIM_Power_SRC/GPIO1/PEWake1# | RESERVED/REFCLKP1 | 71 |
| 68 | UIM_Power_SINK/CLKREQ1# | GND | 69 |
| 66 | UIM_SWP/PERST1# | Reserved/PERn1 | 67 |
| 64 | RESERVED | Reserved/PERp1 | 65 |
| 62 | ALERT# (IO)(0.3V) | Reserved/PETn1 | 61 |
| 60 | DC CLK (IO)(0.3V) | Reserved/PETp1 | 59 |
| 58 | QCCDATA (IO)(0.3V) | GND | 57 |
| 56 | WL_DISABLE1# (IO)(0.3V) | PEWake0# (IO)(0.3V) | 55 |
| 54 | Reserves/W_DISABLE2 (IO)(0.3V) | CLKREQ0# (IO)(0.3V) | 53 |
| 52 | PERST0# (IO)(0.3V) | GND | 51 |
| 50 | SUSCLK(32KHz) (IO)(0.3V) | REFCLKN0 | 49 |
| 48 | COEX1 (IO)(0.18V) | REFCLKP0 | 47 |
| 46 | COEX3 (IO)(0.18V) | PERn0 | 45 |
| 44 | COEX3 (IO)(0.18V) | PERp0 | 43 |
| 42 | VENDOR DEFINED | PERp0 | 41 |
| 40 | VENDOR DEFINED | PETn0 | 39 |
| 38 | VENDOR DEFINED | PETp0 | 37 |
| 36 | UART RTS (IO)(1.8V) | GND | 35 |
| 34 | UART CTS (IO)(1.8V) | GND | 33 |
| 32 | UART Tx (IO)(1.8V) | GND | 31 |
| 30 | UART Rx (IO)(1.8V) | GND | 29 |
| 28 | UART Wake# (IO)(0.3V) | GND | 27 |
| 26 | GND | GND | 25 |
| 24 | LED#2 (IO)(0.1V) | GND | 23 |
| 22 | PCM_OUT/IS2_SD_OUT (IO)(0.18V) | GND | 21 |
| 20 | PCM_IN/IS2_SD_IN (IO)(0.18V) | GND | 19 |
| 18 | PCM_SYNC/IS2_WS (IO)(0.18V) | GND | 17 |
| 16 | PCM_CLK/IS2_SCK (IO)(0.18V) | GND | 15 |
| 14 | LED#1 (IO)(0.1V) | GND | 13 |
| 12 | LED#1 (IO)(0.1V) | GND | 11 |
| 10 | LED#1 (IO)(0.1V) | GND | 9 |
| 8 | LED#1 (IO)(0.1V) | GND | 7 |
| 6 | LED#1 (IO)(0.1V) | GND | 5 |
| 4 | 3.3V | USB_D+ | 3 |
| 2 | 3.3V | USB_D- | 1 |

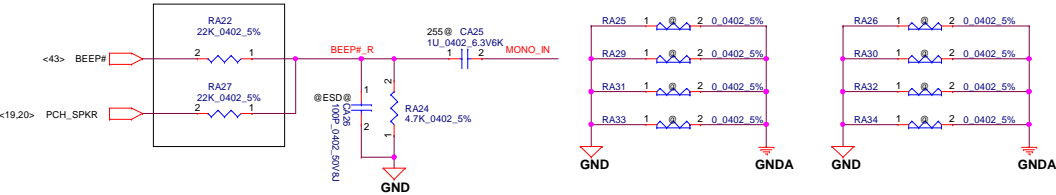
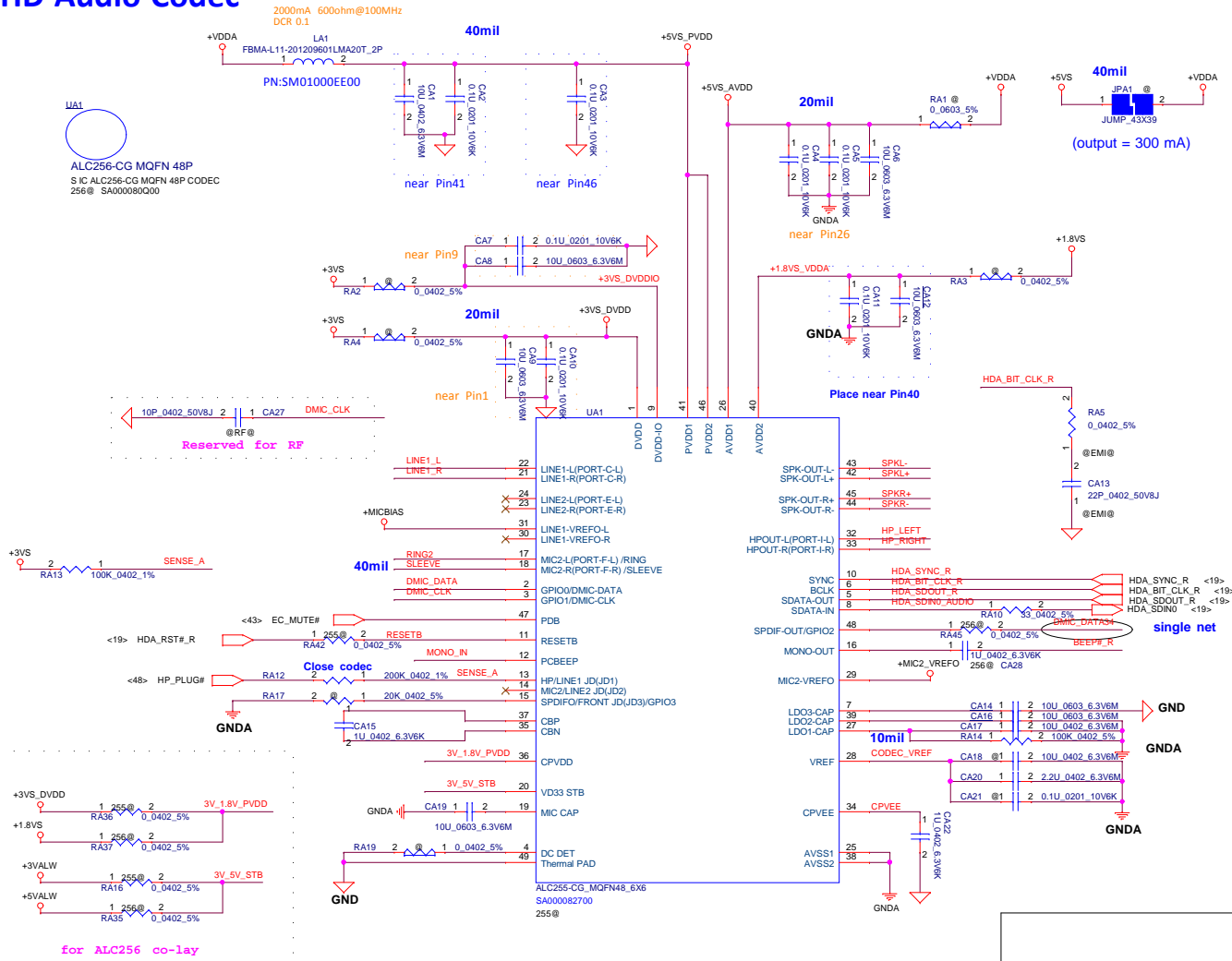
(link to PICE Port 15)
PCI_E X1
(From PCH CLKOUT2)
PCI_E CLK



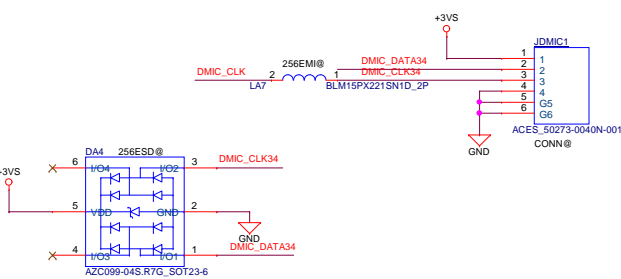
For CNVi Card

| | | | | | |
|---|--|----------------------------|--|--------------------------|--|
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| Custom | | Document Number | | 1.A | |
| Date: | | Tuesday, February 13, 2018 | | Sheet 41 of 73 | |

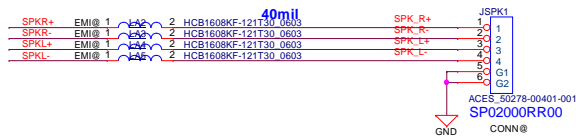
HD Audio Codec



DMIC3/4 Conn. (support on 256)

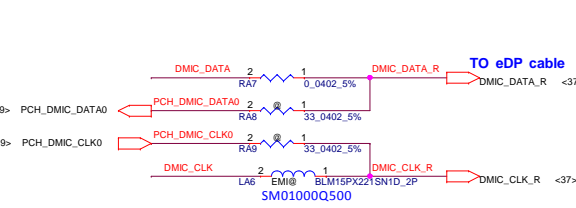


Int. Speaker Conn.

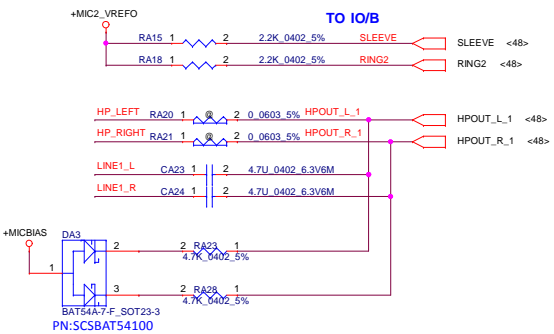


Digital MIC

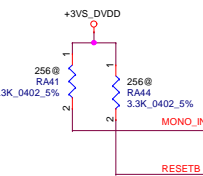
MIC BOM upload by Audio Team



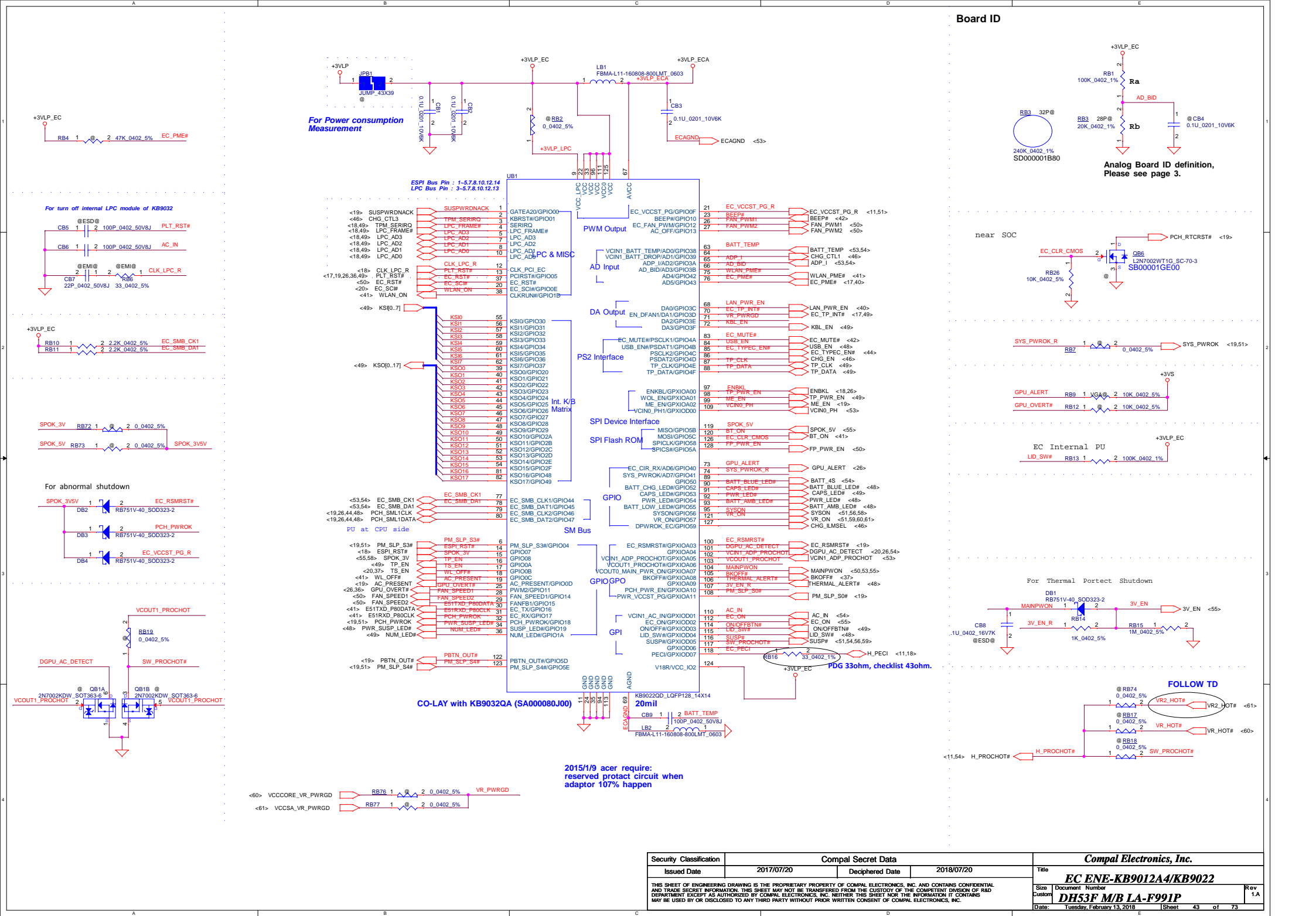
Headphone Out

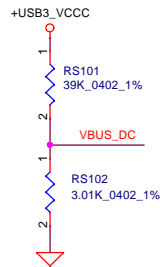
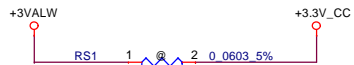
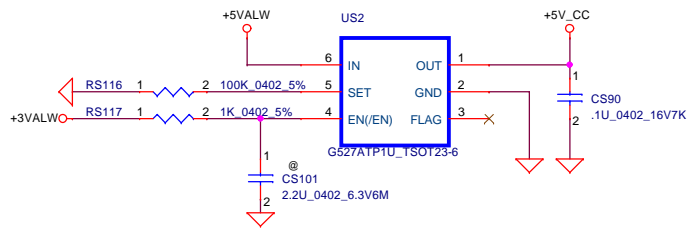


I2C for Co-lay ALC255



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| Size | Document Number | Rev | | Date | |
| Custom | DH53F M/B LA-F991P | 1.A | | Tuesday, February 13, 2018 | |
| Sheet | | 42 | | of | |
| Date | | 13 | | 2018 | |



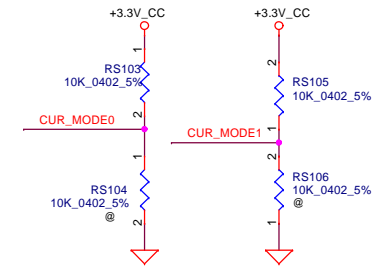
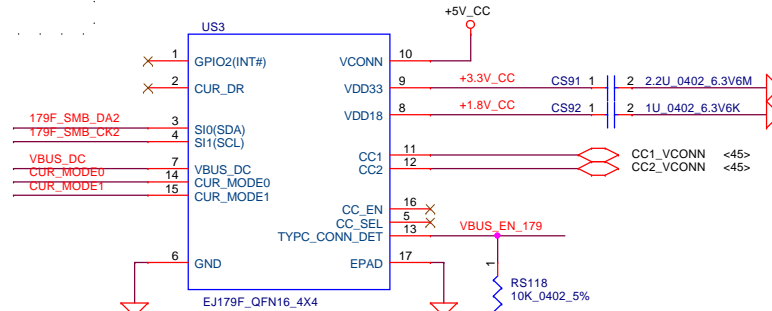


Scaled input
for detection of VBUS DC levels

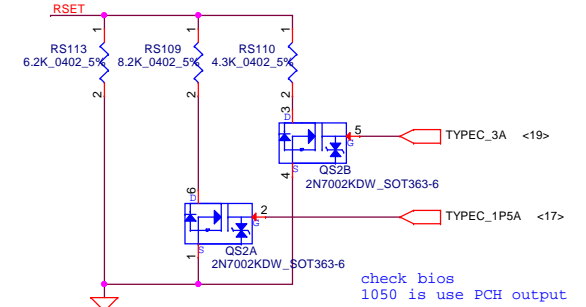
Remove INT#,
platform doesn't monitor it

CC_SEL
report CC1 or CC2 is connection

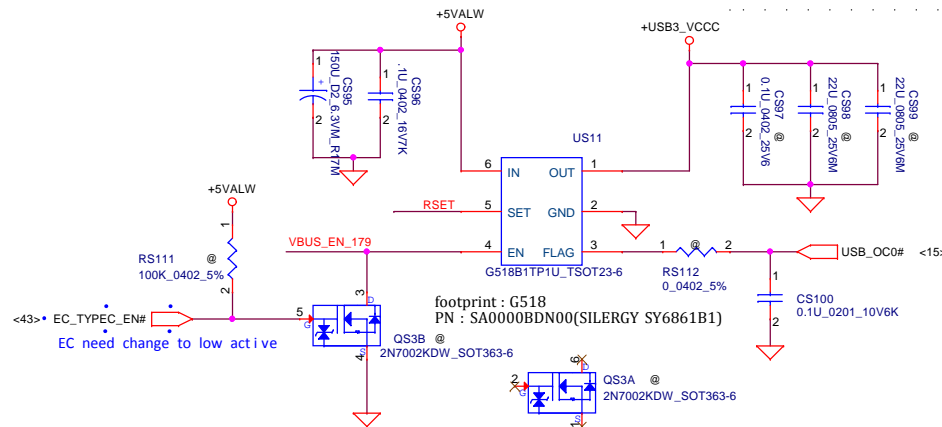
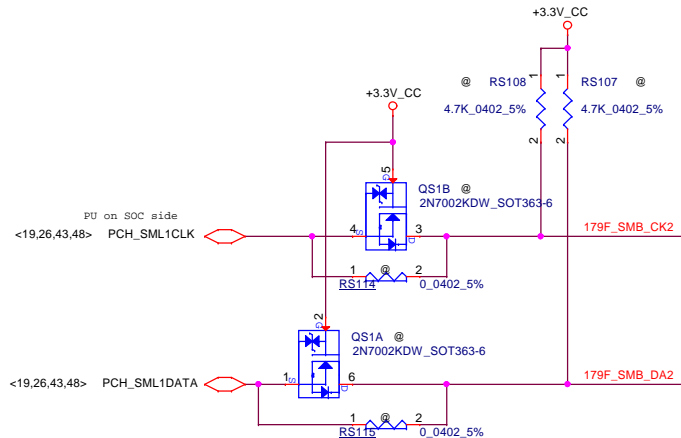
CC_EN
power path control "low active"



| Initial Current mode selection | | |
|--------------------------------|-----------|-----------------|
| CUR_MODE0 | CUR_MODE1 | MODE |
| H | L | Default Current |
| L | H | Medium current |
| H | H | High current |



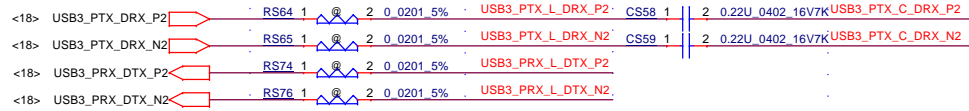
| G518 MOS Current Limit | | | | |
|------------------------|----------------------|----------|------|-------------|
| GPP_B1 (TYPEC_1P5A) | GPP_B4 (TYPEC_3A) | RSET(kΩ) | MODE | limit point |
| L | L | 6.2 | 0.9A | 1.09A |
| L | H | 3.53 | 1.5A | 1.92A |
| H | L | 2.54 | 2A | 2.67A |
| *H | H | 1.94 | 3A | 3.5A |



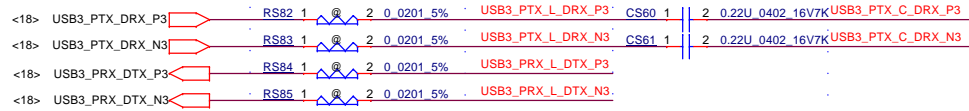
| Initial Current mode selection | | |
|--------------------------------|---------------|-------|
| VBUS_EN_179 | EC_TYPPEC_EN# | V BUS |
| L | H | 0 |
| L | L | 0 |
| H | H | 0 |
| H | L | 1 |

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|---|----------------------------|--------------------|------------|--------------------------|----|
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| Size | Document | Number | Rev | DH53F M/B LA-F991P | |
| Custom | | | | 1.A | |
| Date: | Tuesday, February 13, 2018 | Sheet | 44 | of | 73 |

USB3.0 (Port 2)

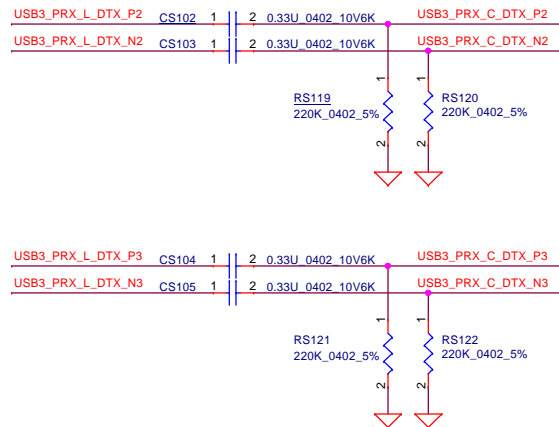
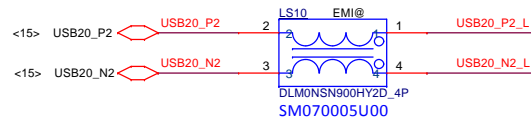


USB3.0 (Port 3)



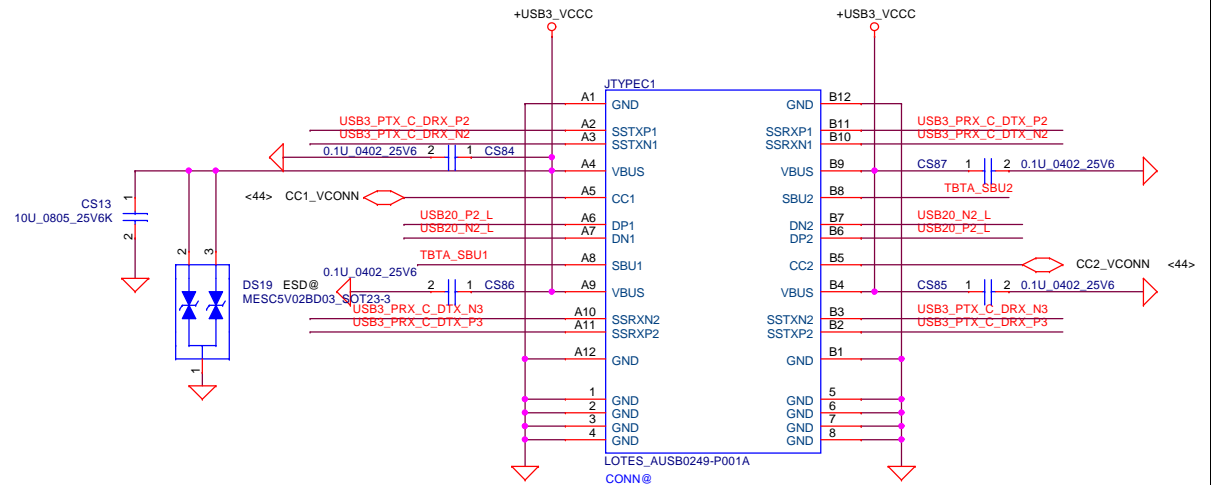
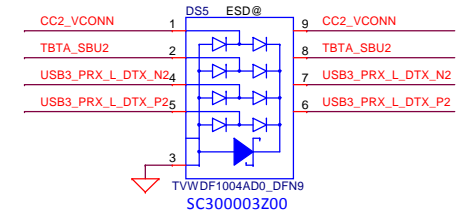
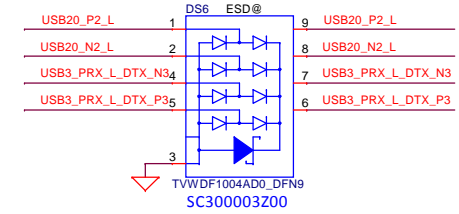
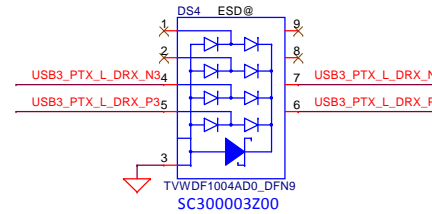
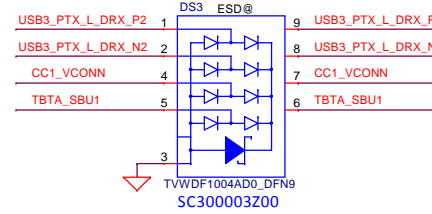
Change to 0201 for placement.

Follow intel #575549.



Follow intel #575549 for ESD/EOS protection.

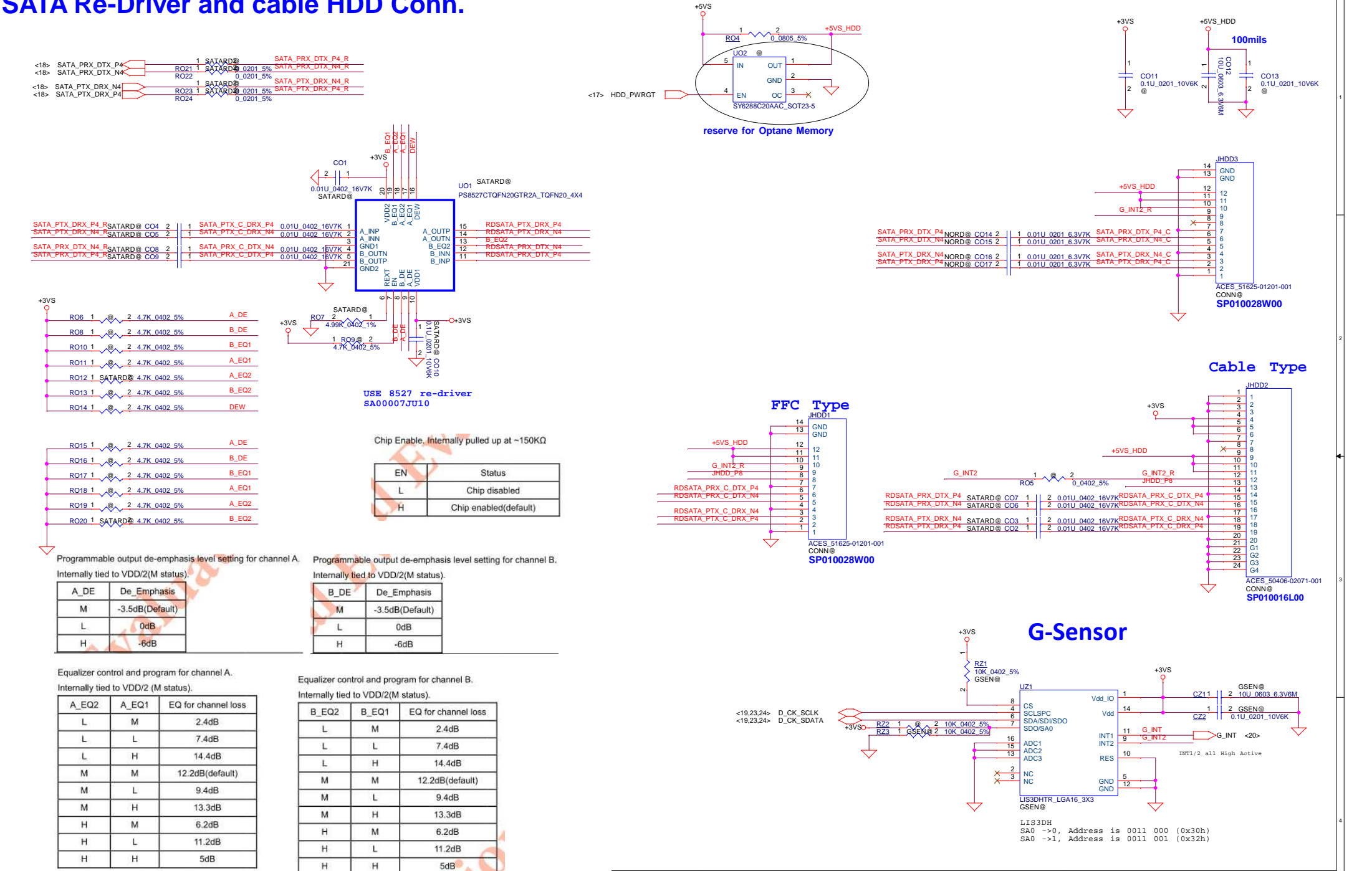
For ESD request



CC1_VCONN & CC2_VCONN need 20mil trace width.

| | | | | | |
|---|----------------------------|--------------------|--------------------|--------------------------|---------|
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| Size | Custom | Document Number | DH53F M/B LA-F991P | | Rev 1.A |
| Date: | Tuesday, February 13, 2018 | Sheet | 45 | of | 73 |

SATA Re-Driver and cable HDD Conn.



Chip Enable. Internally pulled up at ~150KΩ

| EN | Status |
|----|-----------------------|
| L | Chip disabled |
| H | Chip enabled(default) |

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

| A_DE | De_Emphasis |
|------|-----------------|
| M | -3.5dB(Default) |
| L | 0dB |
| H | -6dB |

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

| B_DE | De_Emphasis |
|------|-----------------|
| M | -3.5dB(Default) |
| L | 0dB |
| H | -6dB |

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

| A_EQ2 | A_EQ1 | EQ for channel loss |
|-------|-------|---------------------|
| L | M | 2.4dB |
| L | L | 7.4dB |
| L | H | 14.4dB |
| M | M | 12.2dB(default) |
| M | L | 9.4dB |
| M | H | 13.3dB |
| H | M | 6.2dB |
| H | L | 11.2dB |
| H | H | 5dB |

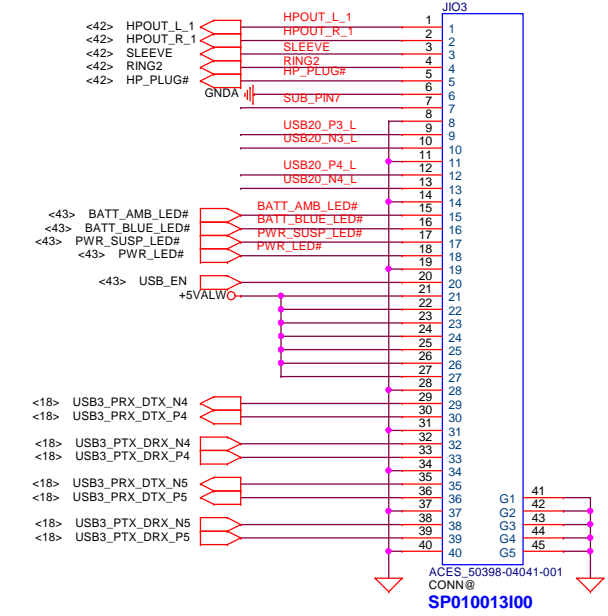
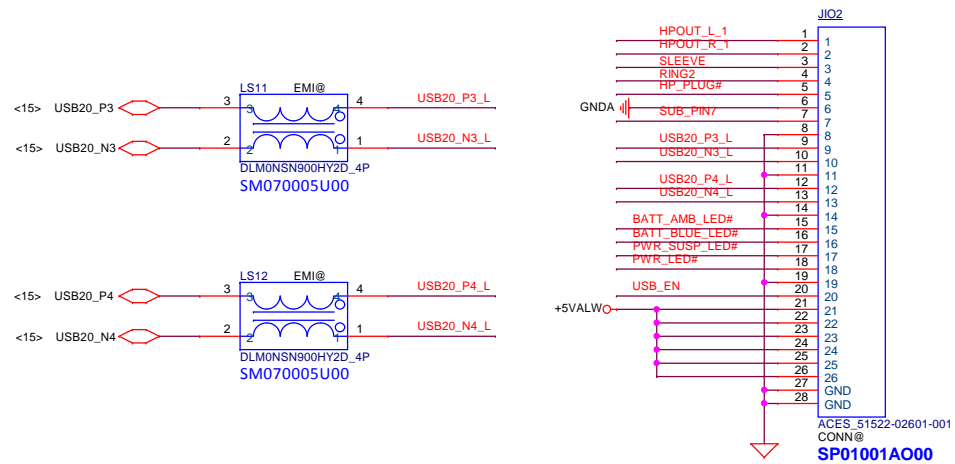
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

| B_EQ2 | B_EQ1 | EQ for channel loss |
|-------|-------|---------------------|
| L | M | 2.4dB |
| L | L | 7.4dB |
| L | H | 14.4dB |
| M | M | 12.2dB(default) |
| M | L | 9.4dB |
| M | H | 13.3dB |
| H | M | 6.2dB |
| H | L | 11.2dB |
| H | H | 5dB |

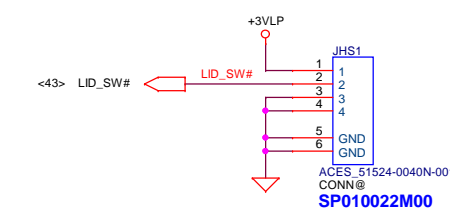
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|-------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|
| Issued Date | 2017/07/20 | Deciphered Date | 2018/07/20 | Title | |
| | | | | HDD/ Re-Driver/ G-sensor | |
| | | | | Size | Document Number |
| | | | | DH53F M/B LA-F991P | |
| | | | | Date: | Tuesday, February 13, 2018 |
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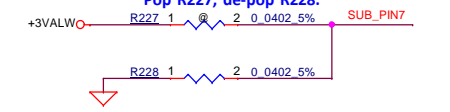
To USB/B FPC BTB CONN



To Hall sensor/B

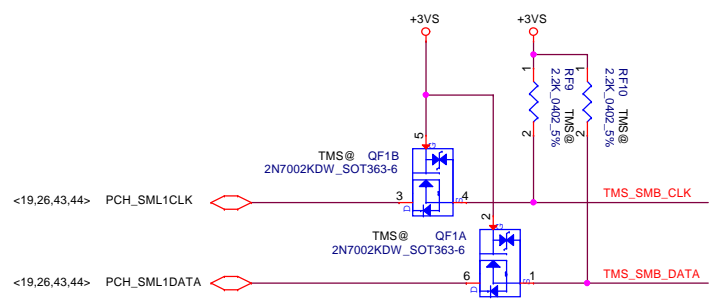
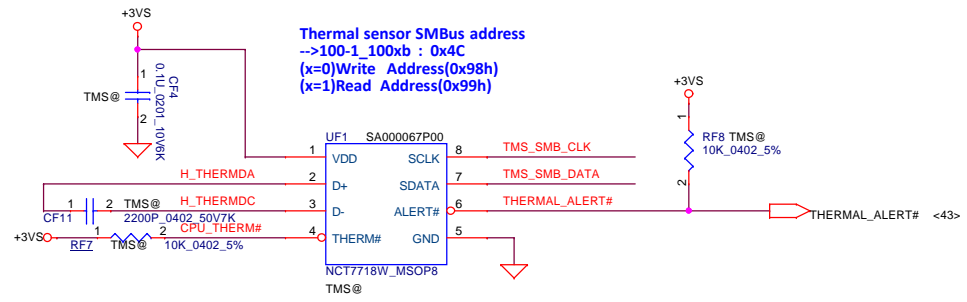


For USB3.0 DB.
Pop R227, de-pop R228.



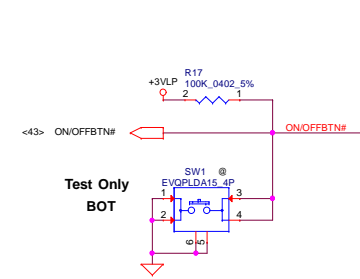
THERMAL SENSOR

Thermal sensor SMBus address
->100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)

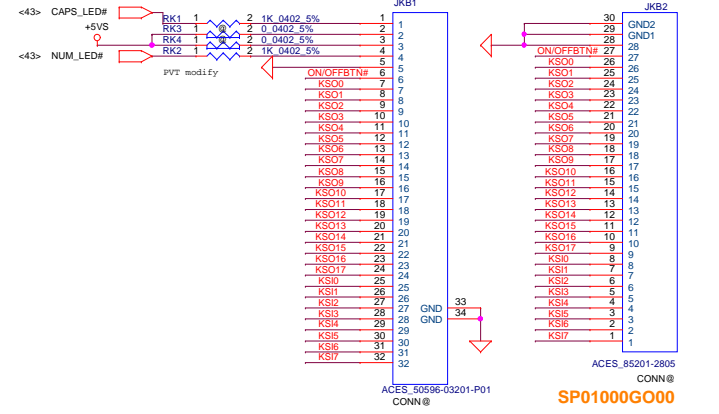


| | | | | | |
|---|----------------------------|--------------------|--------------------|--------------------------|---------|
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| Size | Custom | Document Number | DH53F M/B LA-F991P | | Rev 1.A |
| Date: | Tuesday, February 13, 2018 | Sheet | 48 | of | 73 |

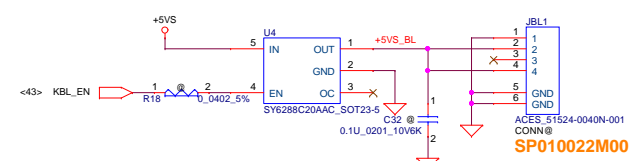
ON/OFF BTN



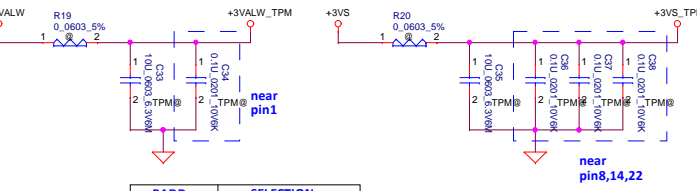
KB Conn.



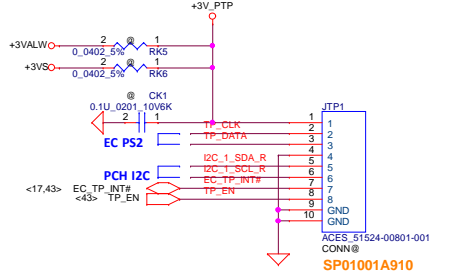
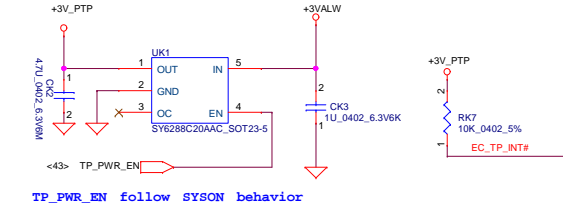
KB BackLight



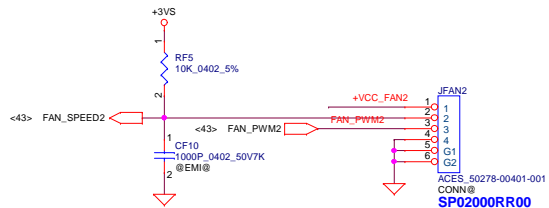
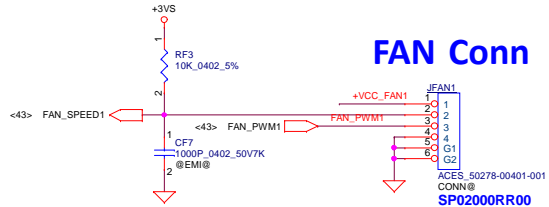
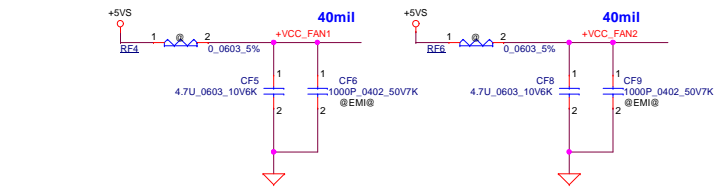
TPM



Touch Pad

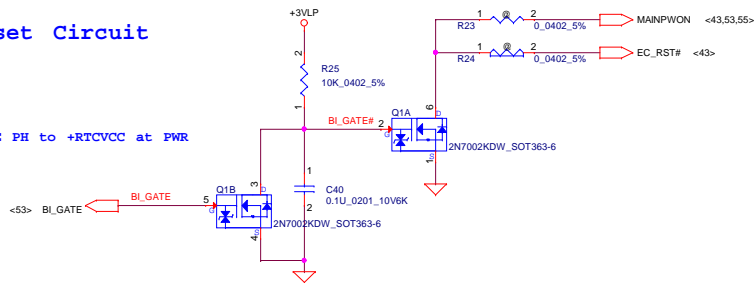


SERIRQ PH 10K to +3VS at PCH side
CLKRUN# PH 10K to +3VS at PCH side
LPCPD# had internal PH

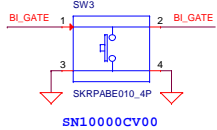


Reset Circuit

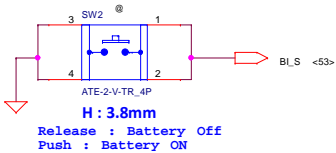
BI_GATE PH to +RTCVCC at PWR side



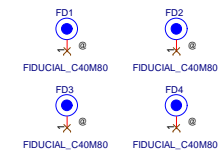
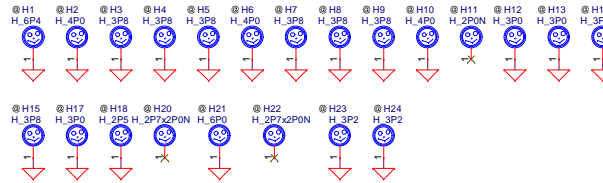
Reset Button



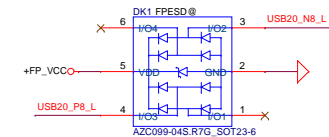
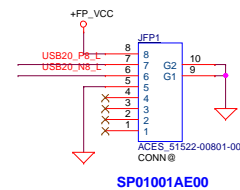
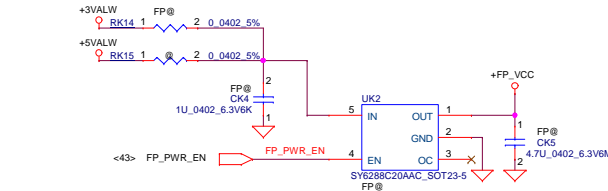
BI SW



Screw Hole



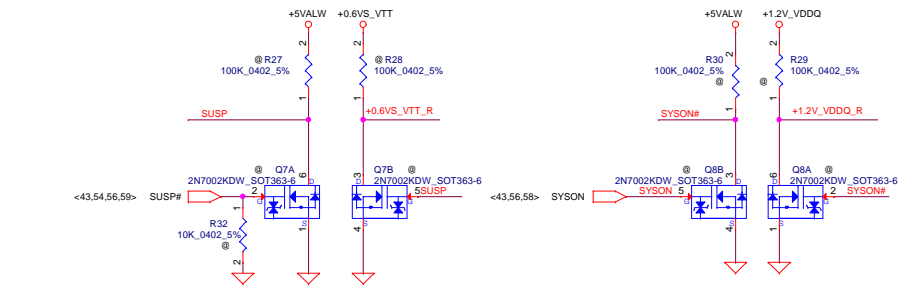
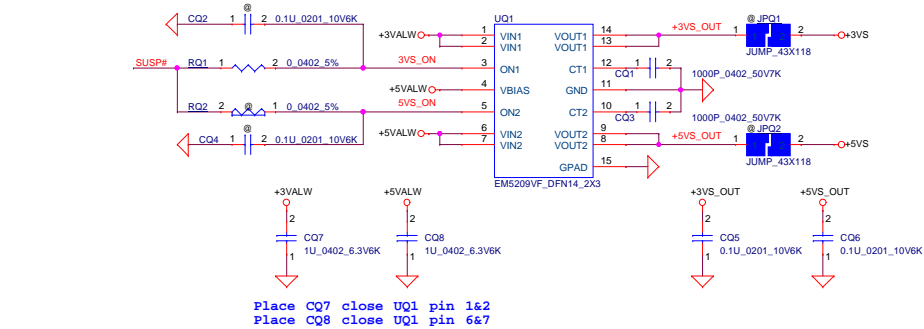
Finger Print



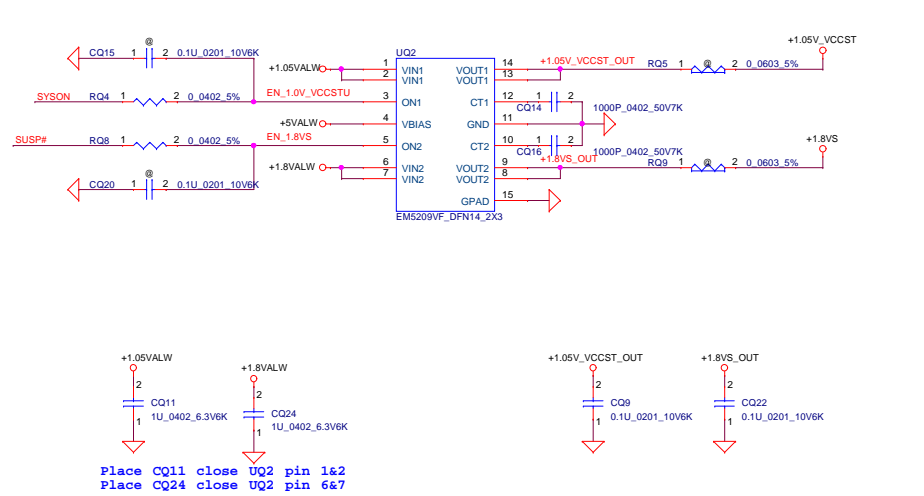
| PIN | ETU801 | FA577E-1200 |
|-----|-------------|-------------|
| 1 | +FP_VCC(5V) | +FP_VCC(3V) |
| 2 | USBP | D+ |
| 3 | USBN | D- |
| 4 | GND | GND |
| 5 | NC | NC |
| 6 | NC | NC |
| 7 | NC | NC |
| 8 | NC | NC |

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| | | | | Custom DH53F M/B LA-F991P Rev 1.A |
| | | | | Date: Tuesday, February 13, 2018 Sheet 50 of 73 |

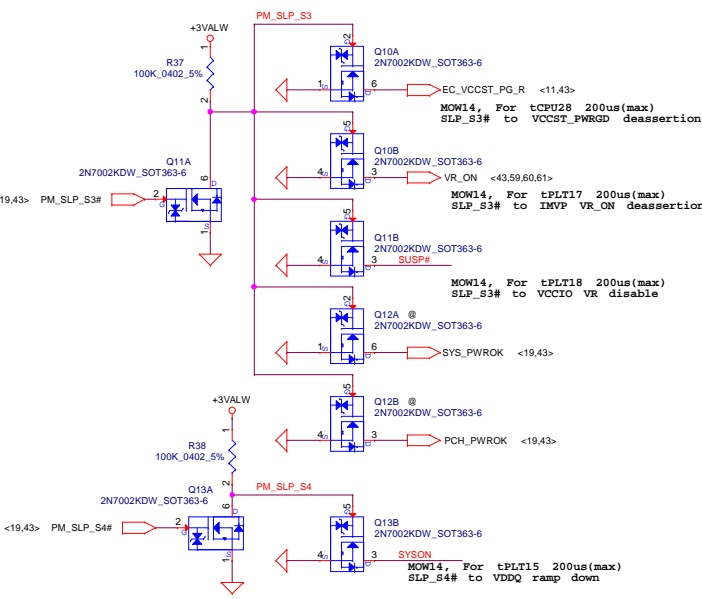
System DC interface



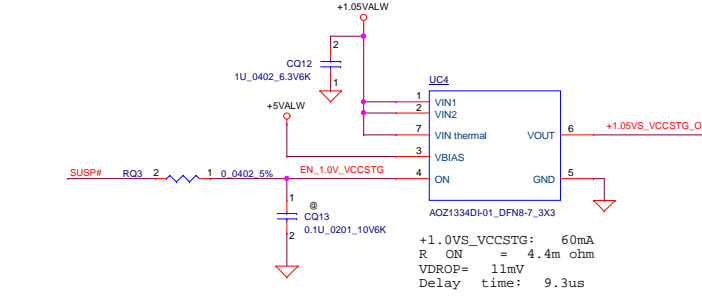
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



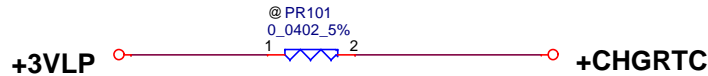
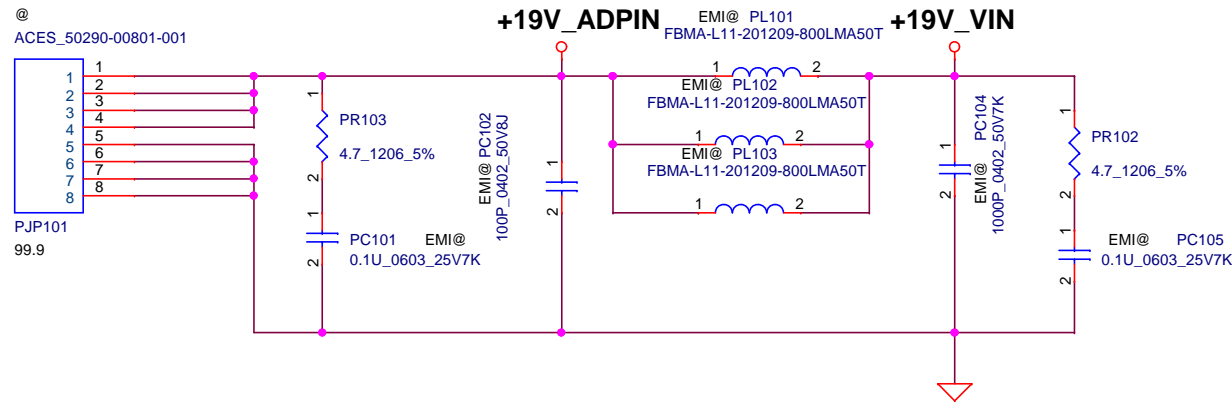
For Power ON/Off Sequence



+1.05VALW TO +1.05VS_VCCSTG



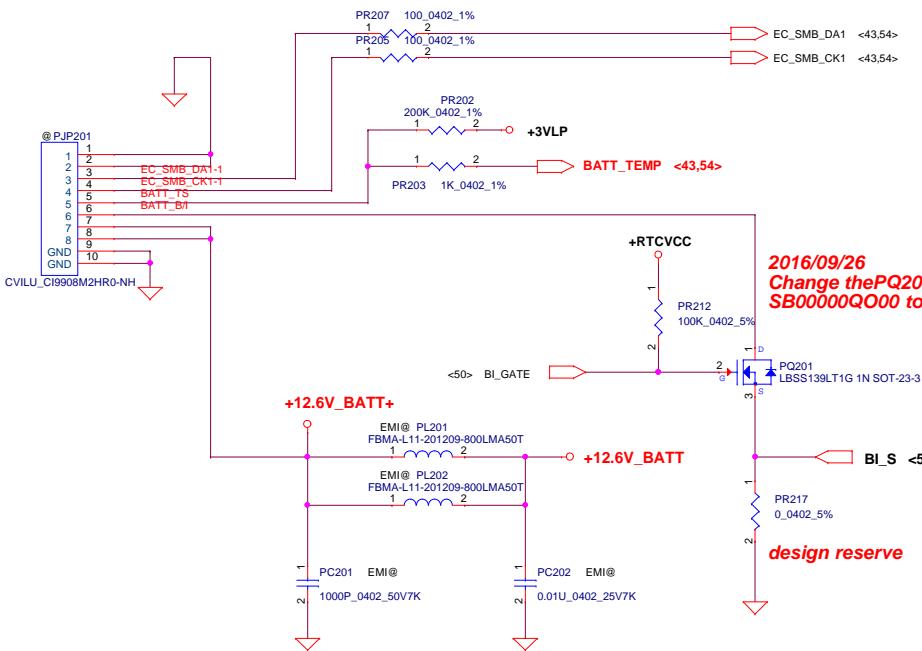
change PL101 PL102 PL103 from
M01000P200 to SM01000U600



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|----------|
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| | | | | Custom | 1.A |
| Date: Tuesday, February 13, 2018 | | | | Sheet | 52 of 73 |

Battery Bot Side

- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TEMP
- PIN6 BI
- PIN7 Batt+
- PIN8 Batt+



2016/09/26
Change thePQ201 from
SB00000Q000 to SB00001GD00,

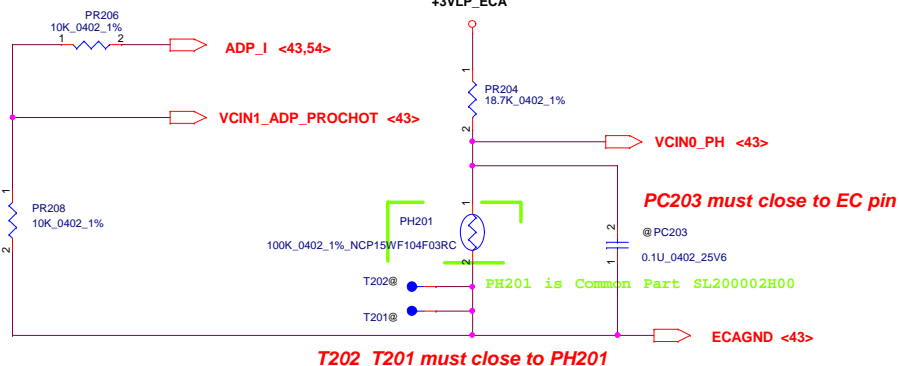
2016/11/22 update

| For KB9022 sense 5mΩ | Active | Recovery |
|-------------------------|--------|----------|
| | | |
| | | |

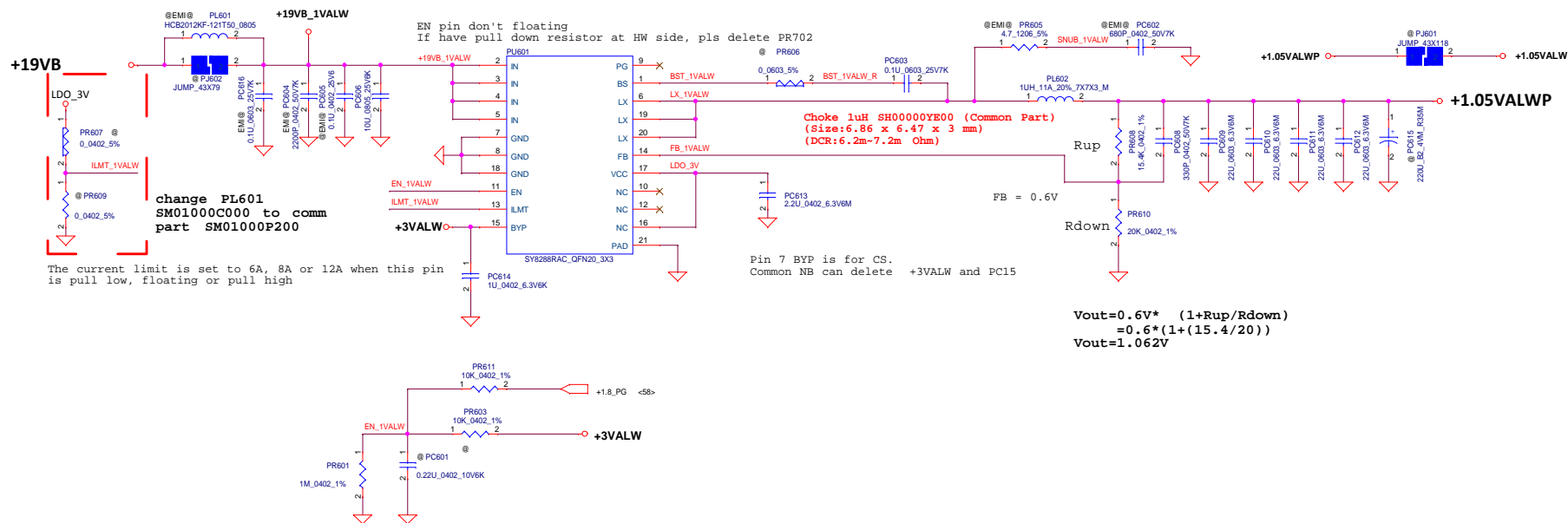
When PR204=16.9K

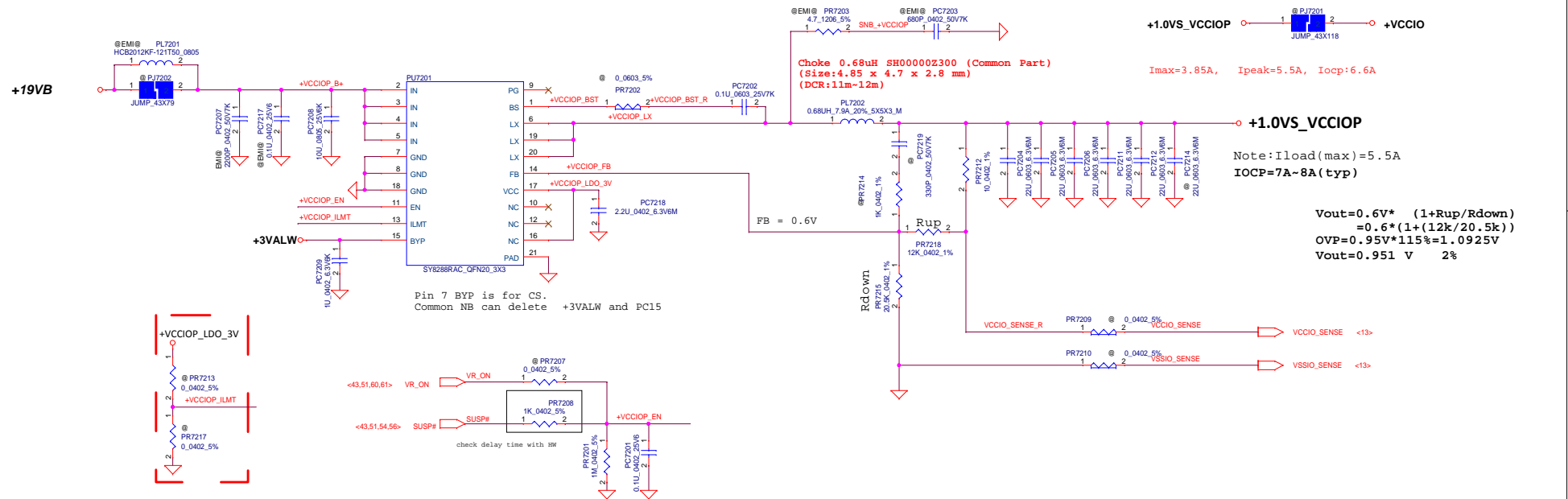
| For KB9022 OTP | Active | Recovery |
|-------------------|----------|----------|
| VCIN0_PH(V) | 89°C, 1V | 56°C, 2V |
| PH202(ohm) | 7.3092K | 26.11K |

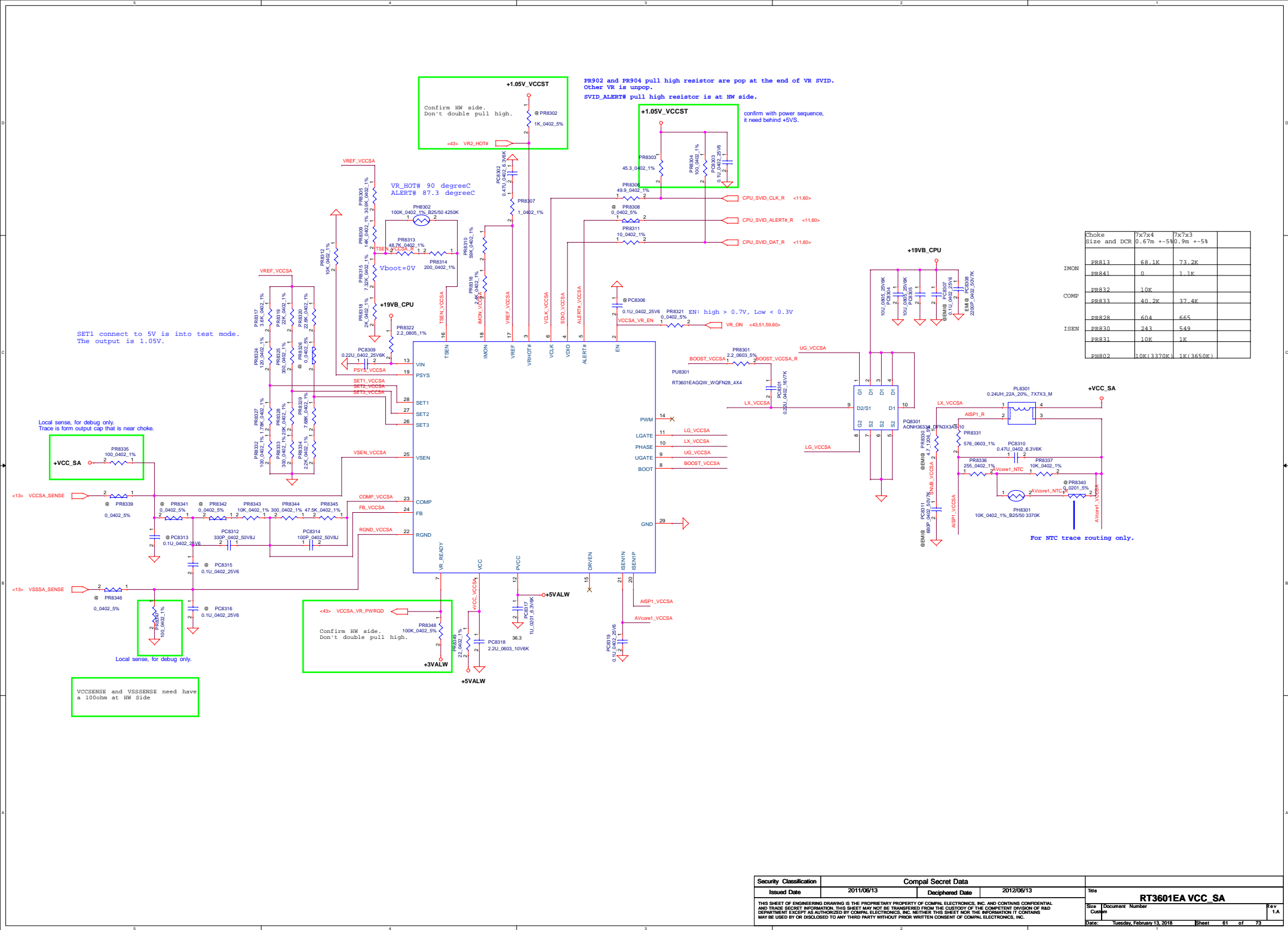
3/27 thermal PH1 92°C ->89°C



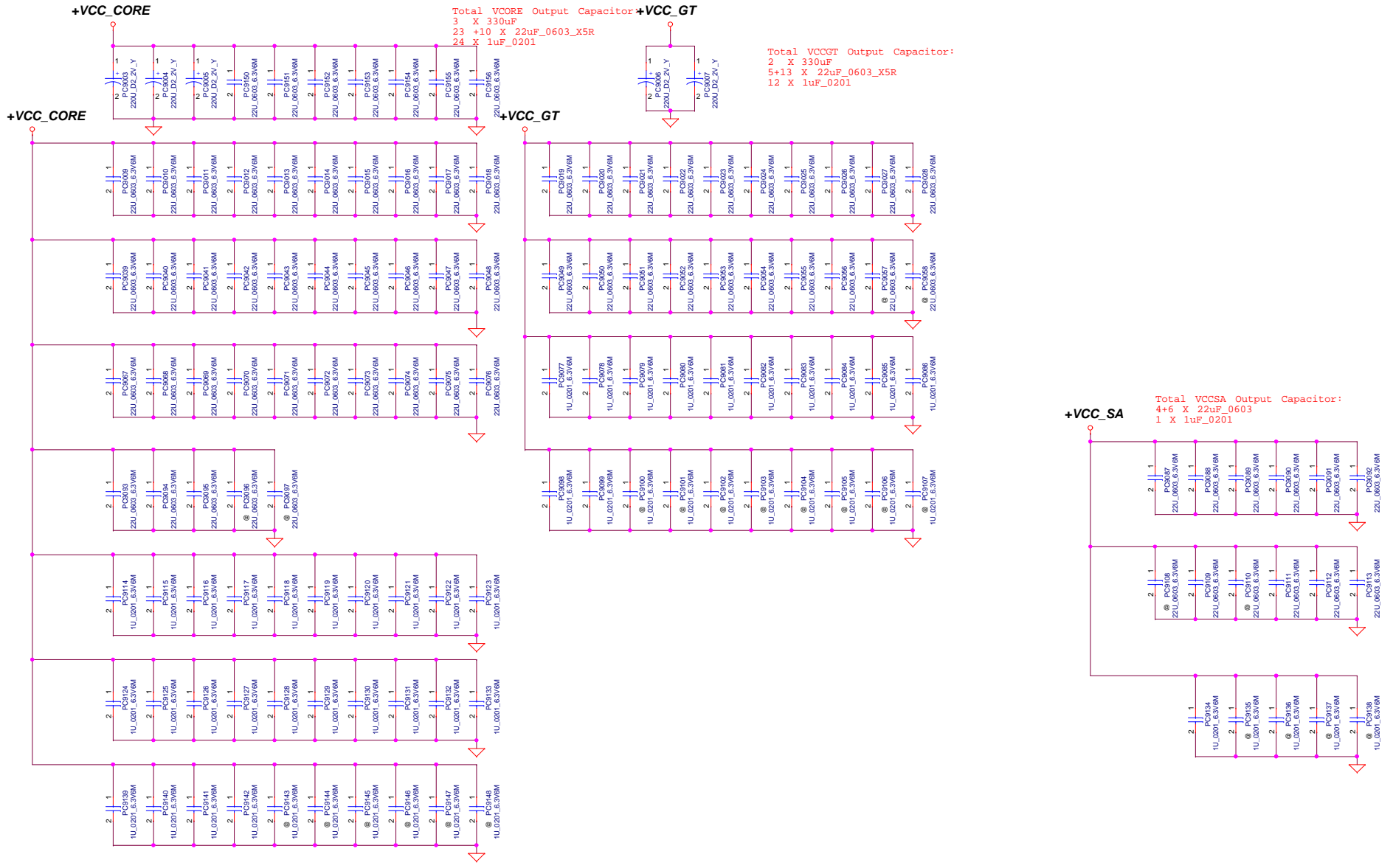
$$ADP_I=20*I(adapter)*0.01$$
$$I(adapter)=adapter(W)*130\%/19$$

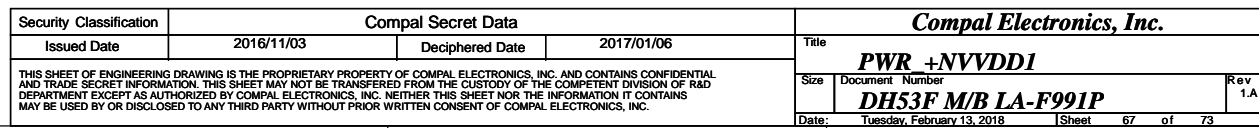


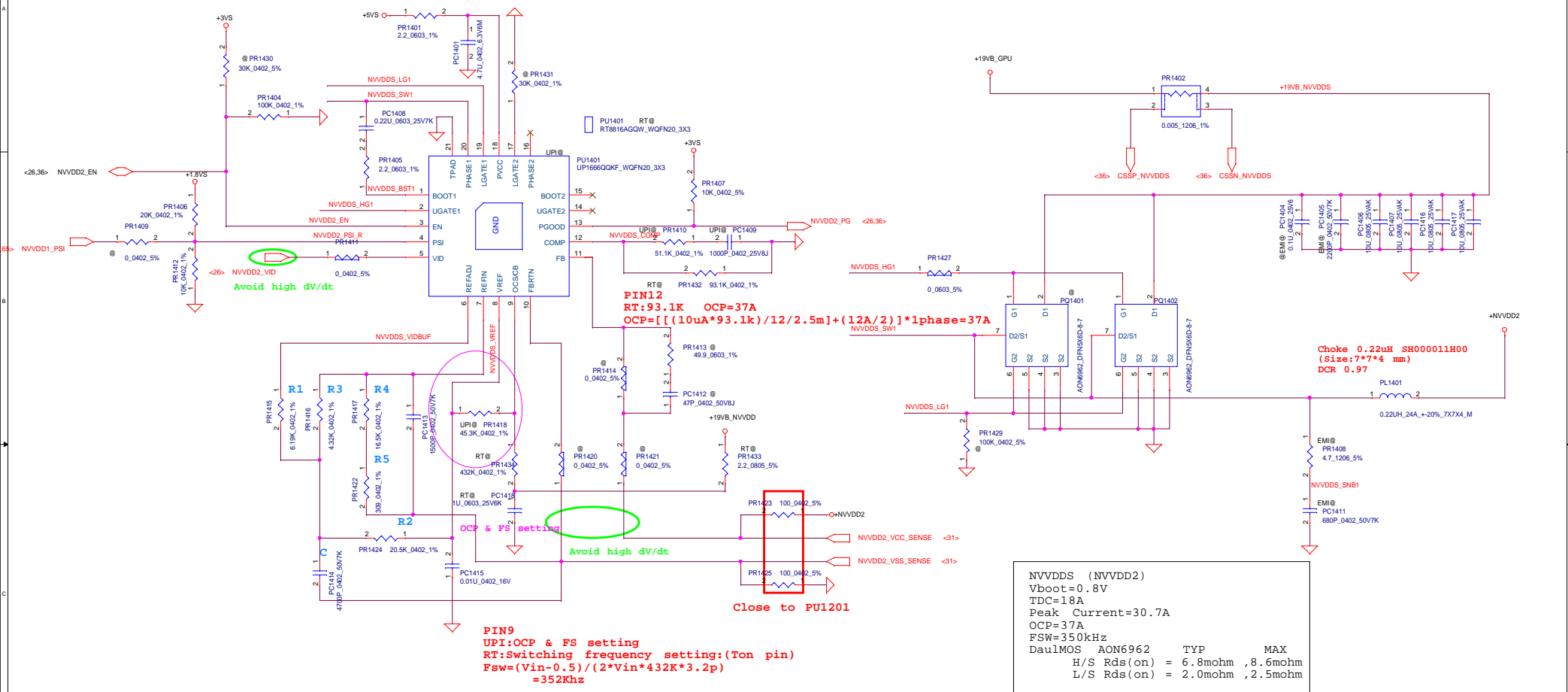




| Choke | Size and DCR | 7x7x4 | 7x7x3 |
|-------|--------------|------------|-----------|
| IMON | | 0.67m +-5% | 0.9m +-5% |
| COMP | | | |
| ISEN | | | |
| PR813 | 68.1K | 73.2K | |
| PR841 | 0 | 1.1K | |
| PR832 | 10K | | |
| PR833 | 40.2K | 37.4K | |
| PR828 | 604 | 665 | |
| PR830 | 243 | 549 | |
| PR831 | 10K | 1K | |
| PR802 | 10K(3370K) | 1K(3650K) | |







| Item | Fixed Issue | Rev. | PG# | Modify List | Date | Phase |
|------|--|------|-----|---|-------|-------|
| 01 | Oohm ->R-Short | 1.0 | | PR326,PR304,PR314,PR316,PR317,PR322,PR333,PR334,PR8111,PR8120,PR8128,PR8129,PR8139,PR8142,PR8143,PR8153,PR8154,PR8155,PR8163,PR8165,PR8170,PR8175,PR8184,PR8190,PR8198,PR8204,PR8308,PR8339,PR8341,PR8342,PR8346,PR8326,PR1414_SD028000080 chage to _R-Short 0402 PR326 0_0603_5%_SD013000080 ->R-Short 0603_SD013000080 | 12/17 | A.2 |
| 02 | material shortage | 1.0 | | PC313,PC314_1U_0402_16V6K_SE000000U00 ->_1U_6.3V_K_X5R_0201_SE000000YB00 PC1303,PC1314,PC1353,PC8101,PC8122,PC8135,PC8150,PC8158 _0.1U_0603_50V7K_SE025104K80 ->_0.1U_25V_K_X7R_0603_SE042104K80 PC305,PC324_0.1U_0402_25V7K_SE000000W210_->_0.1U_0402_25V6_SE000000G880 | 12/17 | A.2 |
| | Acer SW2 design reserve | 1.0 | | PR217 0_0402_5%_SD028000080(unpop) -> SMT 0402_SD028000080 | 12/17 | A.2 |
| 03 | For 4S per cell 4.35V battery | 1.0 | | PQ307_LMUN5113T1G_SOT323-3_SB000013X00_->del PR327unpop_0_0603_5%_SD013000080_->del PR342Add_->_2M_0402_1%_SD034200480 PR343Add_100K_0402_1%_SD034100380 PQ315Add_2N7002KW_SOT323-3_SB000005T00 | 12/20 | A.2 |
| 04 | charger boost cap to 0.47uF but material shortage so down size. | 1.0 | | PC309_0.22U_0603_25V7K_SE0000005Z80_->_0.47U_0402_16V4Z_SE0000002F80 | 12/21 | A.2 |
| 05 | ACDET change | 1.0 | | PR306_392K_0402_1%_SD034392380_->_499K_0402_1%_SD034499380 PR310_52.3K_0402_1%_SD034523280_->_66.5K_0402_1%_SD034665280 | 12/28 | A.2 |

| | | | | | |
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| | | | | Size: Custom Document Number: DH53FM/BLA-F991P Rev: 1.A | |
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|------|-------|------------|-------|---------------------------------|---|-------|------|
| 1 | 46 | USB | 10/18 | Correct USB charger connection. | 1.Change RS15 connection to CHG_ILMSEL. | DVT | 0.2 |
| 2 | 19,36 | Placement | 10/18 | Placement | 1.Remove RPH10, add RH197,RH198. 2.UG27 source change to +1.8VALW for +1.8VSDGPU_AON/+1.8VSDGPU_MAIN. | DVT | 0.2 |
| 3 | 41 | CNVI | 10/18 | For CNVI power rail. | 1.Co-lay RM46 for CNVI +3VALW power rail. | DVT | 0.2 |
| 4 | 42 | Material | 10/18 | X1 code issue. | 1.LA1 change to SM01000NS00. | DVT | 0.2 |
| 5 | 48 | USB | 10/18 | redriver verify. | 1.Add one USB3.0 port to JIO3. | DVT | 0.2 |
| 6 | | Placement | 10/21 | Placement | 1. Change RM36,RM37,RM42,RM43 to 0402 size. 2. Change RH186,RH47,RH98~RH100,RH103,RH105,RD2,RD3,RD6,RD13,RD15,RD17,RM34,RM35,RM38,RM39,RS1,R19,R20,RQ5,RQ6,RQ9 to R-short. 3. Change RS8,RS10 to 1206 R-short. 4. Change RH97 to 0805 R-short. | DVT | 0.2 |
| 7 | 11 | ESD cap. | 10/21 | Sourcer request. | 1.Change CC66,CC68 to SE074102K80. | DVT | 0.2 |
| 8 | 43 | EC | 10/21 | EC board ID. | 1.Change RB3 to 12kohm/28P@ and 160kohm/32P@ | DVT | 0.2 |
| 9 | | Cap. | 10/24 | Sourcer request. | 1. Change CA6,CA8,CA9,CA12,CA14,CA16,CA19,CC71~CC81,CC88~CC90,CG130,CG131,CG143~CG145,CG168,CG169,CG178~CG181,CG193,CG205~CG207,CG229,CG230,CG241,CG243,CG253~CG255,CG267~CG269,CG291,CG292,CG303~CG305,CX1,CX3 from 0402 to 0603 size. | DVT | 0.2 |
| 10 | 50 | Screw hole | 10/25 | Screw hole | 1.Change H21 footprint to H_6P0. | DVT | 0.2 |
| 11 | 48 | USB EMI | 10/25 | EMI issue. | 1.Add LS11,LS12. | DVT | 0.2 |
| 12 | 41,43 | CNVI | 10/26 | For CNVI power rail detect. | 1.Add net CNVI_DET#,RB78,RB79. | DVT | 0.2 |
| 13 | 46 | USB | 10/26 | Correct USB charger connection. | 1.Correct USB2.0 connection for US12. | DVT | 0.2 |
| 14 | 42 | DMIC | 10/26 | Acer request. | 1.Change JDMIC1 from 8pin to 4pin. | DVT | 0.2 |
| 15 | 47 | SATA | 11/03 | Co-layout. | 1.Co-lay JHDD3,CO14~CO17,RO21~EO24. | DVT | 0.2 |
| 16 | 44 | SMBus | 11/08 | Co-layout. | 1.Co-lay RS114,RS115. | DVT | 0.2 |
| 17 | 49 | SW | 11/14 | Remove debug SW. | 1.De-pop SW1. | DVT | 0.2 |
| 18 | 44 | Type-C | 11/14 | CC logic control by EC SMBus. | 1.De-pop QS1,QS3,RS107,RS108,RS111. Pop RS114,RS115. | DVT | 0.2 |
| 19 | 16 | Cap. | 11/14 | by crystal vendor test result. | 1.Change CH7,CH8 to 10pF. | DVT | 0.2 |
| 20 | 45 | Cap. | 11/16 | For shortage. | 1.Change CS84~CS87 to SE00000G880. | DVT | 0.2 |
| 21 | 43 | CNVI | 11/16 | CNVI detect by SW. | 1.De-pop RB78. Pop RB79. | DVT | 0.2 |
| 22 | 43 | CNVI | 12/15 | Remove CNVI detect. | 1.Remove RB78, RB79 and netname CNVI_DET#. | PVT | 1.0 |
| 23 | 18 | PECI | 12/15 | For Peci issue. | 1.De-pop RH41. | PVT | 1.0 |
| 24 | 50 | BI SW | 12/15 | By customer request. | 1.De-pop SW2. | PVT | 1.0 |
| 25 | 43 | EC | 12/15 | Update EC board ID. | 1.Change RB3 to 15kohm/28P@ and 200kohm/32P@ | PVT | 1.0 |
| 26 | 42 | Inductor | 12/15 | Change source. | 1.Change LA1 to SM01000EE00. | PVT | 1.0 |
| 27 | | NPI | 12/15 | For NPI test. | 1.Change RB19,RC17,RG143,RG200,RG202,RH101,RH102,RH5,RH6,RH92,RH93,RH94,RH96,RM2,RS114,RS115,RB72,RB76,RL1,RL13,RQ2 to R-short. | PVT | 1.0 |

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| 28 | 44 | Type-C | 12/18 | Change current limit solution | 1.Change US2 to SA00006Y700. 2.Add RS116,RS117,RS118. Reserve CS101. | PVT | 1.0 |
| 29 | 43 | EC | 12/20 | For PWR BATT_4S | 1.Add net BATT_4S to EC pin89. | PVT | 1.0 |
| 30 | 41 | WLAN | 12/20 | For CNVi BT_ON | 1.Add RM47. | PVT | 1.0 |
| 31 | 21 | PCH | 12/20 | For intel sensitive net | 1.Pop CH29,CH34,CS100. | PVT | 1.0 |
| 32 | 45 | Type-C | 12/21 | For intel new topology | 1.Change RS64,RS65,RS74,RS76,RS82~RS85 to 0201 size. 2.Add CS102~CS105,RS119~RS122. | PVT | 1.0 |
| 33 | 36 | GPU | 12/21 | Fine tune GPU sequence | 1.Change CG315 to 0.22uF, RG190 to 16.9k ohm, add RG225. | PVT | 1.0 |
| 34 | 20 | | 12/28 | For MB ID | 1.De-pop RH86. Pop RH85,RH87. | PVT | 1.0 |
| 35 | 7,15 | CPU,PCH | 12/28 | Update intel chip to QS PN | 1.SA0000BPJ10 for i5@, SA0000BPI10 for i7@, SA0000BPF10 for PCH@. | PVT | 1.0 |
| 36 | 7 | DAZ | 12/28 | Update MB DAZ PN. | 1.DAZ29000100 for PCB@. | PVT | 1.0 |
| 37 | 37 | eDP | 12/28 | For eDP sequence | 1.Pop RX1. | PVT | 1.0 |
| 38 | 18,39 | PCIE | 01/11 | For IRST support issue. | 1.Change PCIE port17~20 to port 9~12 for PCIE SSD. 2.Change SATA port0A to port4 for SATA HDD. 3.Change SSD_DEVSLP4 to SSD_DEVSLP1. 4.Change SATA_GP4 to SATA_GPI. | PVT | 1.C |
| 39 | 45 | Type-C | 01/11 | For intel new topology | 1.Place CS58~CS61 close to connector and change net name. | PVT | 1.C |
| 40 | 43 | EC | 01/11 | Update EC board ID. | 1.Change RB3 to 20kohm/28P@ and 240kohm/32P@ | PVT | 1.C |
| 41 | 21 | PCH | 01/12 | For layout routing. | 1.Change RH93 to 0ohm footprint. | PVT | 1.C |
| 42 | 45 | Type-C | 01/16 | For intel new topology | 1.Change CS58~CS61 to 0.22uF. | PVT | 1.C |
| 43 | 7 | CPU,DAZ | 01/27 | Update CPU,DAZ PN | 1.SA0000BPZ10 for i7@, DAZ29000103 for PCB@. | PVT | 1.C |
| 44 | 7,15 | CPU,PCH | 02/13 | Update CPU,PCH PN to MP PN. | 1.SA0000BPJ40 for i5@,SA0000BPZ40 for i7@,SA0000BVP10 for PCH@. | Pre-MP | 1.C |

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